



Software-Defined Radio Handbook

13th Edition

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Products

Complementary Products

Applications

by

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Preface

SDR (Software-Defined Radio) has revolutionized electronic systems for a variety of applications including communications, data acquisition and signal processing.

This handbook shows how DDCs (Digital Downconverters) and DUCs (Digital Upconverters), the fundamental building blocks of SDR, can replace legacy analog receiver and transmitter designs while offering significant benefits in performance, density and cost.

In order to fully appreciate the benefits of SDR, conventional analog receiver and transmitter systems will be compared to their digital counterparts, highlighting similarities and differences.

The inner workings of the SDR will be explored with an in-depth description of the internal structure and the devices used. Finally, some actual board- and system-level implementations and available off-the-shelf SDR products and applications based on such products will be presented.

For more information on complementary subjects, the reader is referred to these Pentek Handbooks:

[Critical Techniques for High-Speed A/D Converters in Real-Time Systems](#)

[High-Speed Switched Serial Fabrics Improve System Design](#)

[Putting FPGAs to Work in Software Radio Systems](#)

[High-Speed, Real-Time Recording Systems](#)

[Putting VPX and OpenVPX to Work](#)

Sampling

Nyquist's Theorem and Sampling

Before we look at SDR and its various implementations in embedded systems, we'll review a theorem fundamental to sampled data systems such as those encountered in Software-Defined Radios.

Nyquist's Theorem:

*"Any signal can be represented by discrete samples if the sampling frequency is at least twice the **bandwidth** of the signal."*

Notice that we highlighted the word bandwidth rather than frequency. In what follows, we'll attempt to show the implications of this theorem and the correct interpretation of sampling frequency, also known as sampling rate.

A Simple Technique to Visualize Sampling

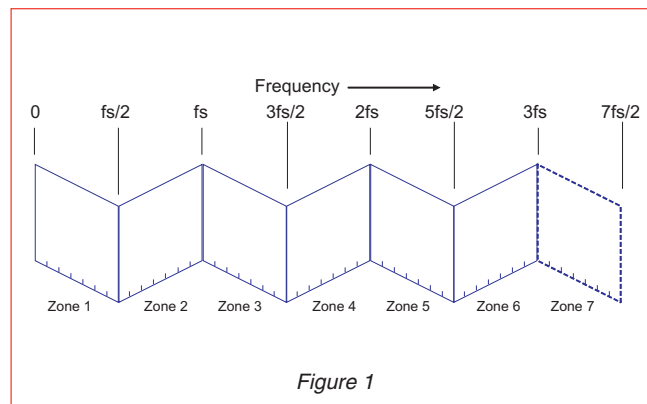
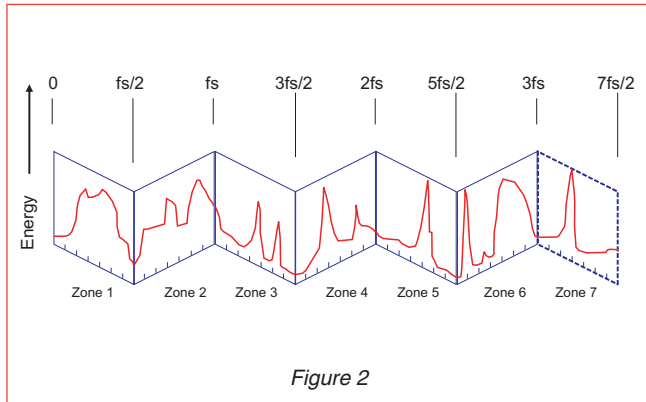


Figure 1

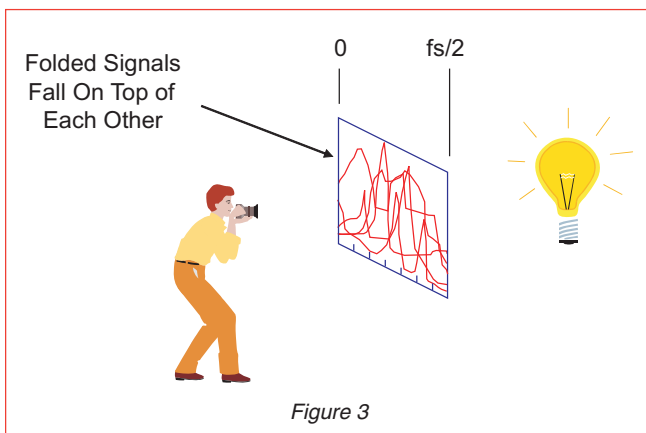
To visualize what happens in sampling, imagine that you are using transparent "fan-fold" computer paper. Use the horizontal edge of the paper as the frequency axis and scale it so that the paper folds line up with integer multiples of one-half of the sampling frequency f_s . Each sheet of paper now represent what we will call a "Nyquist Zone", as shown in Figure 1.

Sampling

Sampling Basics



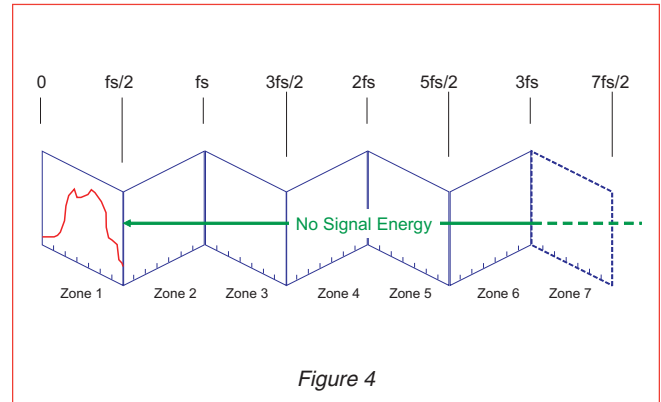
Use the vertical axis of the fan-fold paper for signal energy and plot the frequency spectrum of the signal to be sampled, as shown in Figure 2. To see the effects of sampling, collapse the transparent fan-fold paper into a stack.



The resulting spectrum can be seen by holding the transparent stack up to a light and looking through it. You can see that signals on all of the sheets or zones are “folded” or “aliased” on top of each other — and they can no longer be separated.

Once this folding or aliasing occurs during sampling, the resulting sampled data is corrupted and can never be recovered. The term “aliasing” is appropriate because after sampling, a signal from one of the higher zones now appears to be at a different frequency.

Baseband Sampling



A baseband signal has frequency components that start at $f = 0$ and extend up to some maximum frequency.

To prevent data destruction when sampling a baseband signal, make sure that all the signal energy falls ONLY in the 1st Nyquist band, as shown in Figure 4.

There are two ways to do this:

1. Insert a lowpass filter to eliminate all signals above $f_s/2$, or
2. Increase the sampling frequency so all signals present fall below $f_s/2$.

Note that $f_s/2$ is also known as the “folding frequency”.

Sampling Bandpass Signals

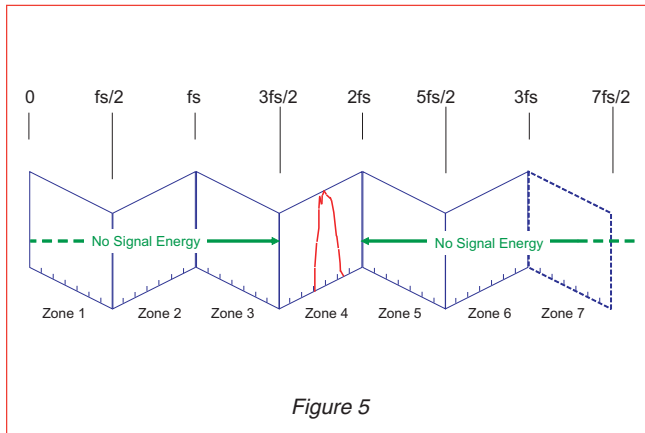
Let’s consider bandpass signals like the IF frequency of a communications receiver that might have a 70 MHz center frequency and 10 MHz bandwidth. In this case, the IF signal contains signal energy from 65 to 75 MHz.

If we follow the baseband sampling rules above, we must sample this signal at twice the highest signal frequency, meaning a sample rate of at least 150 MHz.

However, by taking advantage of a technique called “undersampling”, we can use a much lower sampling rate.

Sampling

Undersampling



Undersampling allows us to use aliasing to our advantage, providing we follow the strict rules of the Nyquist Theorem.

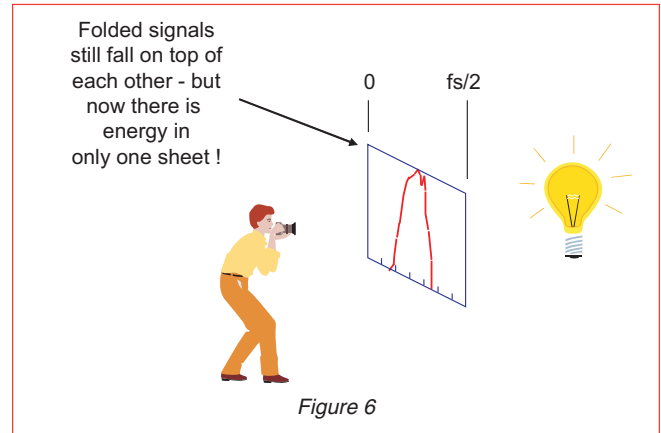
In our previous IF signal example, suppose we try a sampling rate of 40 MHz.

Figure 5 shows a fan-fold paper plot with $F_s = 40$ MHz. You can see that zone 4 extends from 60 MHz to 80 MHz, nicely containing the entire IF signal band of 65 to 75 MHz.

Now when you collapse the fan fold sheets as shown in Figure 6, you can see that the IF signal is preserved after sampling because we have no signal energy in any other zone.

Also note that the odd zones fold with the lower frequency at the left (normal spectrum) and the even zones fold with the lower frequency at the right (reversed spectrum).

In this case, the signals from zone 4 are frequency-reversed. This is usually very easy to accommodate in the following stages of SDR systems.



The major rule to follow for successful undersampling is to make sure all of the energy falls entirely in one Nyquist zone.

There two ways to do this:

1. Insert a bandpass filter to eliminate all signals outside the one Nyquist zone.
2. Increase the sampling frequency so all signals fall entirely within one Nyquist zone.

Summary

Baseband sampling requires the sample frequency to be at least twice the signal bandwidth. This is the same as saying that all of the signals fall within the first Nyquist zone.

In real life, a good rule of thumb is to use the 80% relationship:

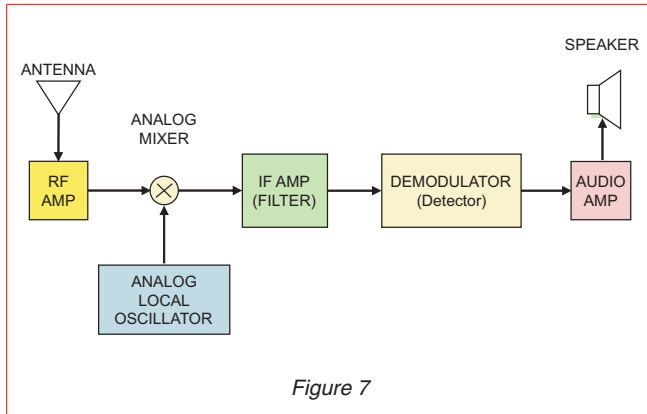
$$\text{Bandwidth} = 0.8 * f_s / 2 = 0.4 * f_s$$

Undersampling allows a lower sample rate even though signal frequencies are high, PROVIDED all of the signal energy falls within one Nyquist zone.

To repeat the Nyquist theorem: The sampling frequency must be at least twice the signal bandwidth — not the signal frequency.

Principles of SDR

Analog Radio Receiver Block Diagram



The conventional heterodyne radio receiver shown in Figure 7, has been in use for nearly a century. Let's review the structure of the analog receiver so comparison to a digital receiver becomes apparent.

First the RF signal from the antenna is amplified, typically with a tuned RF stage that amplifies a region of the frequency band of interest.

This amplified RF signal is then fed into a mixer stage. The other input to the mixer comes from the local oscillator whose frequency is determined by the tuning control of the radio.

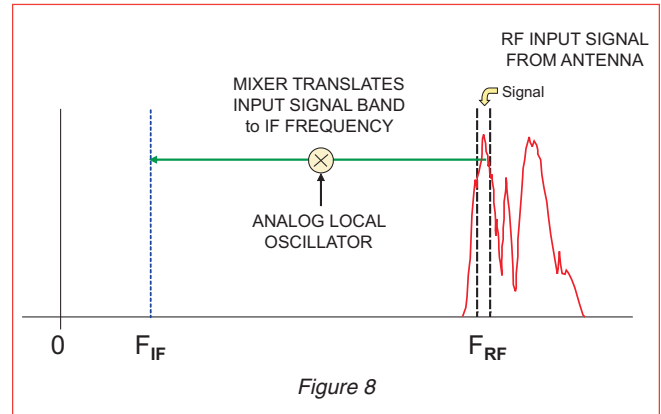
The mixer translates the desired input signal to the IF (Intermediate Frequency) as shown in Figure 8.

The IF stage is a bandpass amplifier that only lets one signal or radio station through. Common center frequencies for IF stages are 455 kHz and 10.7 MHz for commercial AM and FM broadcasts.

The demodulator recovers the original modulating signal from the IF output using one of several different schemes.

For example, AM uses an envelope detector and FM uses a frequency discriminator. In a typical home radio, the demodulated output is fed to an audio power amplifier which drives a speaker.

Analog Radio Receiver Mixer



The mixer performs an analog multiplication of the two inputs and generates a difference frequency signal.

The frequency of the local oscillator is set so that the difference between the local oscillator frequency and the desired input signal (the radio station you want to receive) equals the IF.

For example, if you wanted to receive an FM station at 100.7 MHz and the IF is 10.7 MHz, you would tune the local oscillator to:

$$100.7 - 10.7 = 90 \text{ MHz}$$

This is called “downconversion” or “translation” because a signal at a high frequency is shifted down to a lower frequency by the mixer.

The IF stage acts as a narrowband filter which only passes a “slice” of the translated RF input. The bandwidth of the IF stage is equal to the bandwidth of the signal (or the “radio station”) that you are trying to receive.

For commercial FM, the bandwidth is about 100 kHz and for AM it is about 5 kHz. This is consistent with channel spacings of 200 kHz and 10 kHz, respectively.

Principles of SDR

SDR Receiver Block Diagram

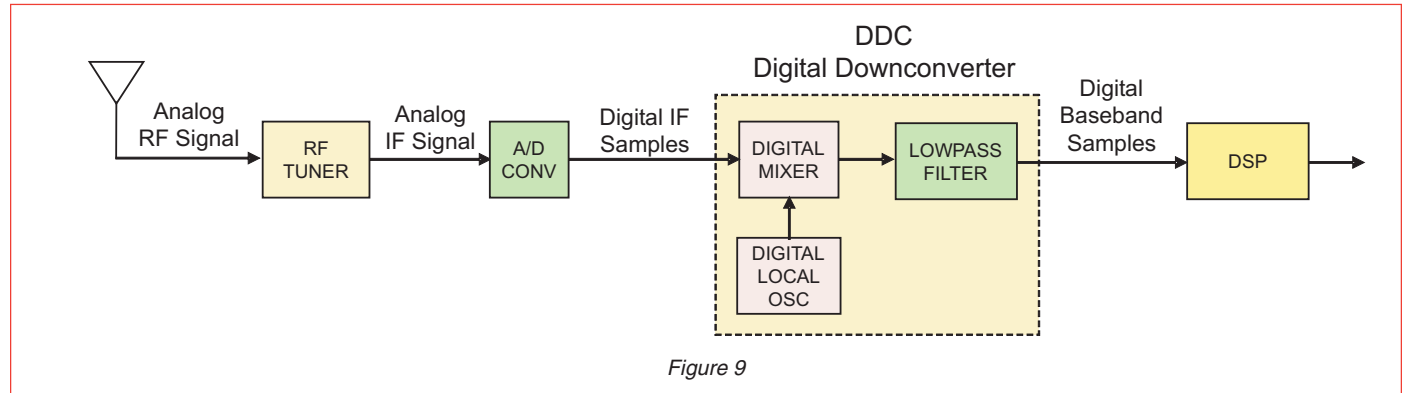


Figure 9 shows a block diagram of a software defined radio receiver. The RF tuner converts analog RF signals to analog IF frequencies, the same as the first three stages of the analog receiver.

The A/D converter that follows digitizes the IF signal thereby converting it into digital samples. These samples are fed to the next stage which is the digital downconverter (DDC) shown within the dotted lines.

The digital downconverter is typically a single monolithic chip or FPGA IP, and it is a key part of the SDR system.

A conventional DDC has three major sections:

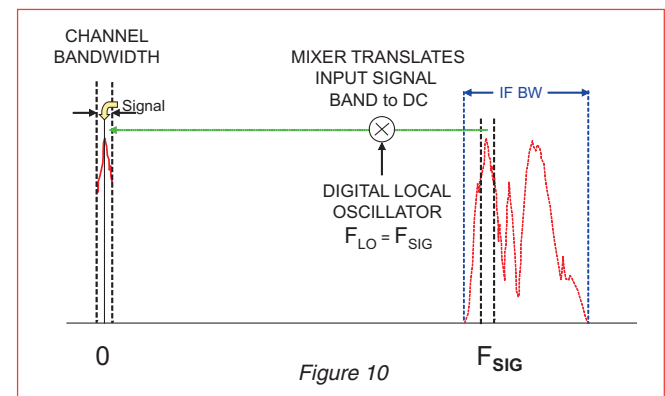
- A digital mixer
- A digital local oscillator
- An FIR lowpass filter

The digital mixer and local oscillator translate the digital IF samples down to baseband. The FIR lowpass filter limits the signal bandwidth and acts as a decimating lowpass filter. The digital downconverter includes a lot of hardware multipliers, adders and shift register memories to get the job done.

The digital baseband samples are then fed to a block labeled DSP which performs tasks such as demodulation, decoding and other processing tasks.

Traditionally, these needs have been handled with dedicated application-specific ICs (ASICs), and program-mable DSPs.

SDR Receiver Mixer



At the output of the mixer, the high frequency wideband signals from the A/D input (shown in Figure 10 above) have been translated down to DC as complex I and Q components with a frequency shift equal to the local oscillator frequency.

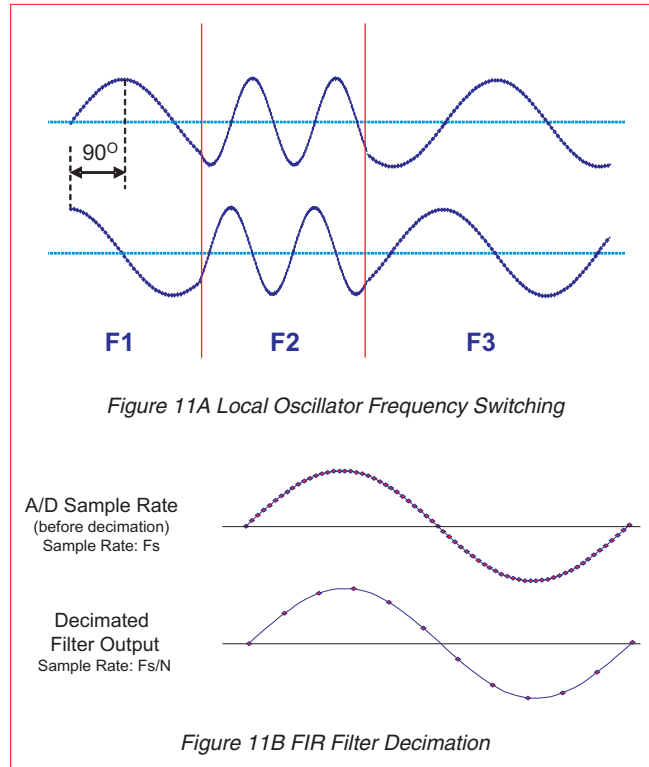
This is similar to the analog receiver mixer except *there*, the mixing was done down to an IF frequency. *Here*, the complex representation of the signal allows us to go right down to DC.

By tuning the local oscillator over its range, any portion of the RF input signal can be mixed down to DC.

In effect, the wideband RF signal spectrum can be “slid” around 0 Hz, left and right, simply by tuning the local oscillator. Note that upper and lower sidebands are preserved.

Principles of SDR

DDC Local Oscillator and Decimation

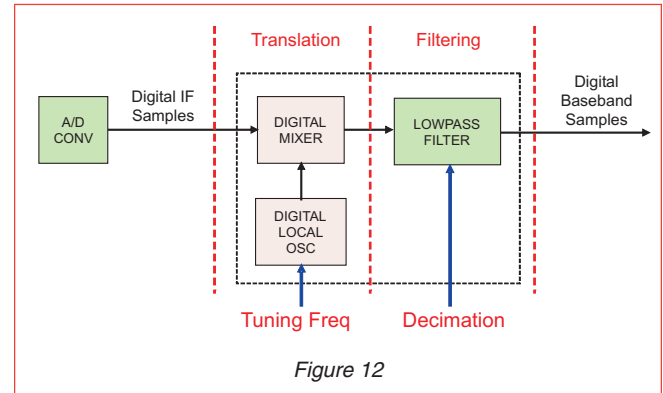


Because the local oscillator uses a digital phase accumulator, it has some very nice features. It switches between frequencies with phase continuity, so you can generate FSK signals or sweeps very precisely with no transients as shown in Figure 11A.

The frequency accuracy and stability are determined entirely by the A/D clock so it's inherently synchronous to the sampling frequency. There is no aging, drift or calibration since it's implemented entirely with digital logic.

Since the output of the FIR filter is band-limited, the Nyquist theorem allows us to lower the sample rate. If we are keeping only one out of every N samples, as shown in Figure 11B above, we have dropped the sampling rate by a factor of N .

DDC Signal Processing



This process is called *decimation* and it means keeping one out of every N signal samples. If the decimated output sample rate is kept higher than twice the output bandwidth, no information is lost.

The clear benefit is that decimated signals can be processed easier, can be transmitted at a lower rate, or stored in less memory. As a result, decimation can dramatically reduce system costs!

As shown in Figure 12, the DDC performs two signal processing operations:

1. Frequency translation with the tuning controlled by the local oscillator.
2. Lowpass filtering with the bandwidth controlled by the decimation setting.

We will next turn our attention to the Software-Defined Radio Transmitter.

Principles of SDR

SDR Transmitter Block Diagram

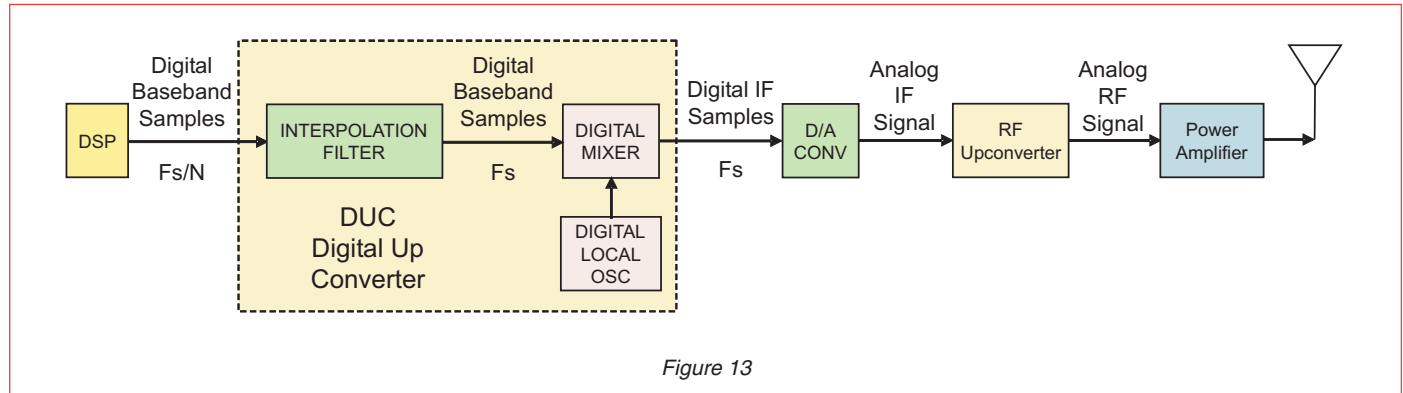


Figure 13

The input to the transmit side of an SDR system is a digital baseband signal, typically generated by a DSP stage as shown in Figure 13 above.

The digital hardware block in the dotted lines is a DUC (digital upconverter) that translates the baseband signal to the IF frequency.

The D/A converter that follows converts the digital IF samples into the analog IF signal.

Next, the RF upconverter converts the analog IF signal to RF frequencies.

Finally, the power amplifier boosts signal energy to the antenna.

DUC Signal Processing

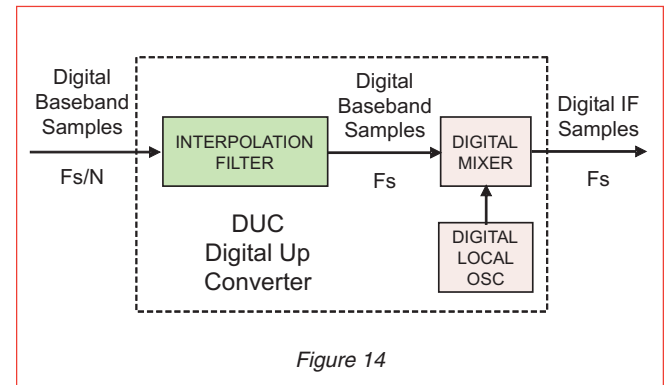


Figure 14

Inside the DUC shown in Figure 14, the digital mixer and local oscillator at the right translate baseband samples up to the IF frequency. The IF translation frequency is determined by the local oscillator.

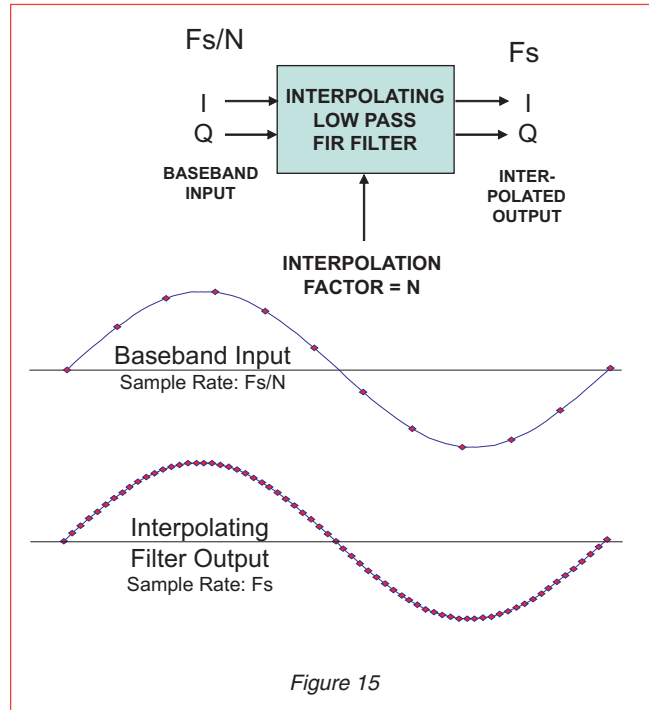
The mixer generates one output sample for each of its two input samples. And, the sample frequency at the mixer output must be equal to the D/A sample frequency f_s .

Therefore, the local oscillator sample rate and the baseband sample rate must be equal to the D/A sample frequency f_s .

The local oscillator already operates at a sample rate of f_s , but the input baseband sample frequency at the left is usually much lower. This problem is solved with the *Interpolation Filter*.

Principles of SDR

Interpolation Filter: Time domain



The interpolation filter must boost the baseband input sample frequency of f_s / N up to the required mixer input and D/A output sample frequency of f_s .

The interpolation filter increases the sample frequency of the baseband input signal by a factor N , known as the interpolation factor.

At the bottom of Figure 15, the effect of the interpolation filter is shown in the time domain.

Notice the baseband signal frequency content is completely preserved by filling in additional samples in the spaces between the original input samples.

The signal processing operation performed by the interpolation filter is the inverse of the decimation filter we discussed previously in the DDC section.

Interpolation Filter: Frequency Domain

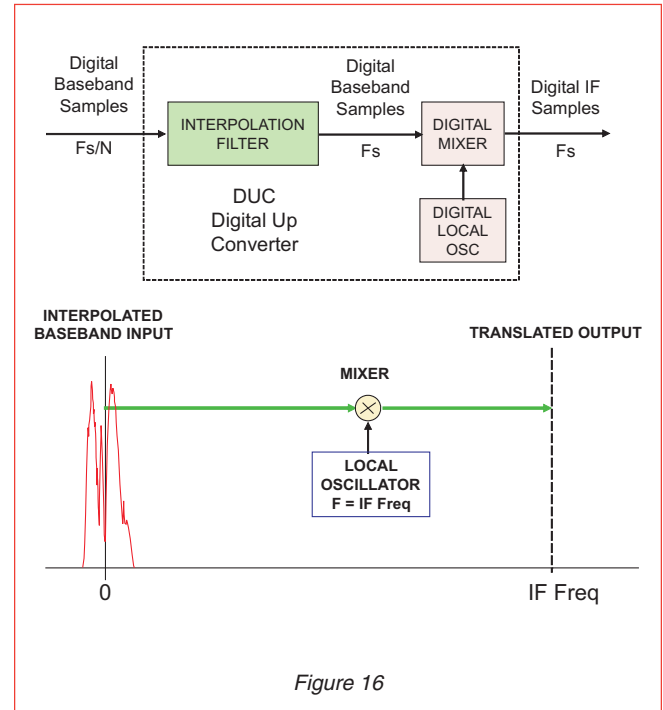


Figure 16 is a frequency domain view of the digital upconversion process.

This is exactly the opposite of the frequency domain view of the DDC in Figure 10.

The local oscillator setting is set equal to the required IF signal frequency, just as with the DDC.

Principles of SDR

DDC Processing

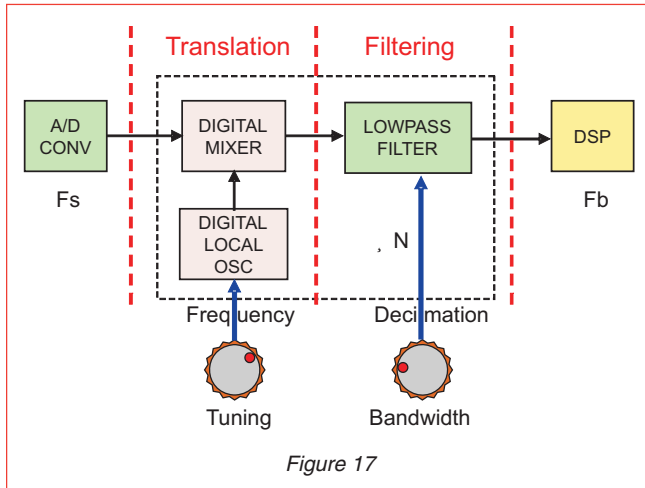


Figure 17

Figure 17 shows the two-step processing performed by the digital downconverter.

Frequency translation from IF down to baseband is performed by the local oscillator and mixer.

The “tuning knob” represents the programmability of the local oscillator frequency to select the desired signal for downconversion to baseband.

The baseband signal bandwidth is set by setting decimation factor N and the lowpass FIR filter:

- Baseband sample frequency $f_b = f_s / N$
- Baseband bandwidth $= 0.8 * f_b$

The baseband bandwidth equation reflects a typical 80% passband characteristic, and complex (I+Q) samples.

The “bandwidth knob” represents the programmability of the decimation factor to select the desired baseband signal bandwidth.

DUC Processing

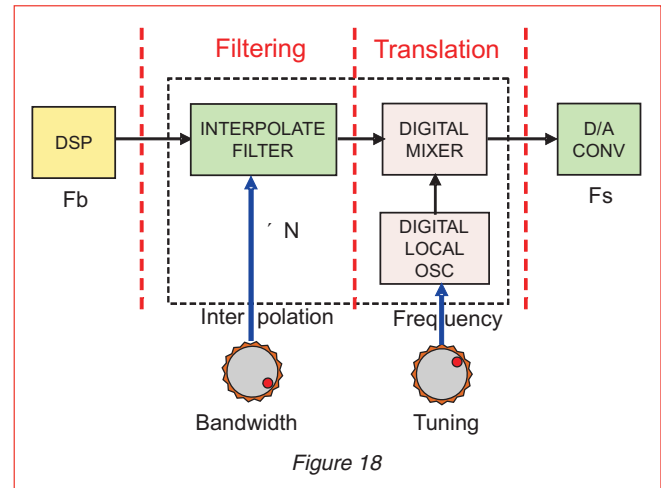


Figure 18

Figure 18 shows the two-step processing performed by the digital upconverter:

The ratio between the required output sample rate and the sample rate input baseband sample rate determines the interpolation factor N .

- Baseband bandwidth $= 0.8 * f_b$
- Output sample frequency $f_s = f_b * N$

Again, the bandwidth equation assumes a complex (I+Q) baseband input and an 80% filter.

The “bandwidth knob” represents the programmability of the interpolation factor to select the desired input baseband signal bandwidth.

Frequency translation from baseband up to IF is performed by the local oscillator and mixer.

The “tuning knob” represents the programmability of the local oscillator frequency to select the desired IF frequency for translation up from baseband.

Principles of SDR

Key DDC and DUC Benefits

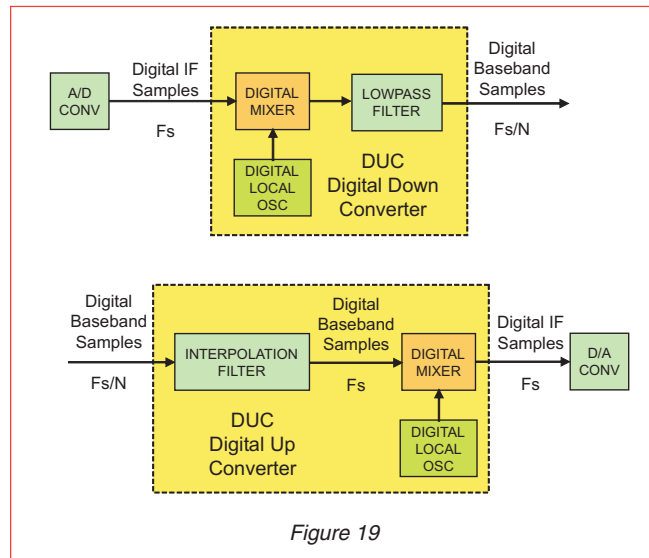


Figure 19

Think of the DDC as a hardware preprocessor for programmable DSP or GPP processor. It preselects only the signals you are interested in and removes all others. This provides an optimum bandwidth and minimum sampling rate into the processor.

The same applies to the DUC. The processor only needs to generate and deliver the baseband signals sampled at the baseband sample rate. The DUC then boosts the sampling rate in the interpolation filter, performs digital frequency translation, and delivers samples to the D/A at a very high sample rate.

The number of processors required in a system is directly proportional to the sampling frequency of input and output data. As a result, by reducing the sampling frequency, you can dramatically reduce the cost and complexity of the programmable DSPs or GPPs in your system.

Not only do DDCs and DUCs reduce the processor workload, the reduction of bandwidth and sampling rate helps save time in data transfers to another subsystem. This helps minimize recording time and disk space, and reduces traffic and bandwidth across communication channels.

SDR Tasks

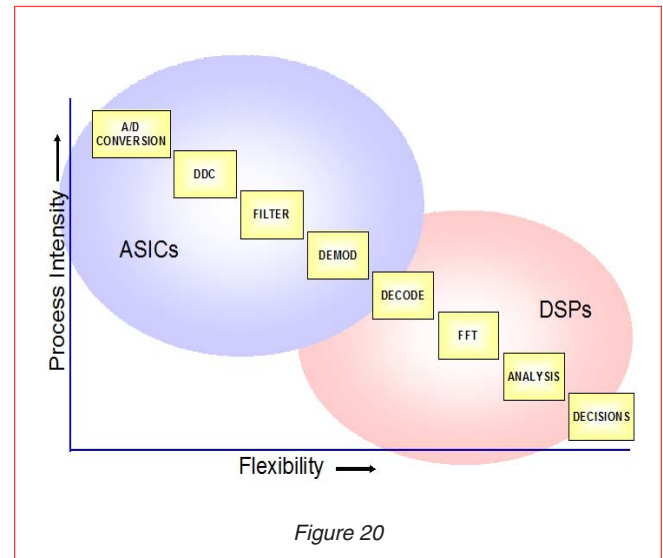


Figure 20

Here we've ranked some of the popular signal processing tasks associated with SDR systems on a two axis graph, with computational Processing Intensity on the vertical axis and Flexibility on the horizontal axis.

What we mean by process intensity is the degree of highly-repetitive and rather primitive operations. At the upper left, are dedicated functions like A/D converters and DDCs that require specialized hardware structures to complete the operations in real time. ASICs are usually chosen for these functions.

Flexibility pertains to the uniqueness or variability of the processing and how likely the function may have to be changed or customized for any specific application. At the lower right are tasks like analysis and decision making which are highly variable and often subjective.

Programmable general-purpose processors or DSPs are usually chosen for these tasks since these tasks can be easily changed by software.

Now let's temporarily step away from the software radio tasks and take a deeper look at programmable logic devices.

FPGA Resources

Early Roles for FPGAs

- Used primarily to replace discrete digital hardware circuitry for:
 - Control logic
 - Glue logic
 - Registers and gates
 - State machines
 - Counters and dividers
- Devices were selected by hardware engineers
- Programmed functions were seldom changed after the design went into production

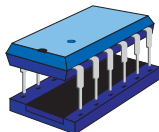


Figure 21

As true programmable gate functions became available in the 1970's, they were used extensively by hardware engineers to replace control logic, registers, gates, and state machines which otherwise would have required many discrete, dedicated ICs.

Often these programmable logic devices were one-time factory-programmed parts that were soldered down and never changed after the design went into production.

Legacy FPGA Design Methodologies

- Tools were oriented to hardware engineers
 - Schematic processors
 - Boolean processors
 - Gates, registers, counters, multipliers
- Successful designs required high-level hardware engineering skills for:
 - Critical paths and propagation delays
 - Pin assignment and pin locking
 - Signal loading and drive capabilities
 - Clock distribution
 - Input signal synchronization and skew analysis



Figure 22

These programmable logic devices were mostly the domain of hardware engineers and the software tools were tailored to meet their needs. You had tools for accepting boolean equations or even schematics to help generate the interconnect pattern for the growing number of gates.

Then, programmable logic vendors started offering predefined logic blocks for flip-flops, registers and counters that gave the engineer a leg up on popular hardware functions.

Nevertheless, the hardware engineer was still intimately involved with testing and evaluating the design using the same skills he needed for testing discrete logic designs. He had to worry about propagation delays, loading, clocking and synchronizing—all tricky problems that usually had to be solved the hard way—with oscilloscopes or logic analyzers.

FPGA Resources

FPGAs: New Device Technology

- ◆ 500+ MHz DSP slices and memory structures
- ◆ Over 3500 dedicated on-chip hardware multipliers
- ◆ On-board GHz serial transceivers
- ◆ Partial reconfigurability maintains operation during changes
- ◆ Switched fabric interface engines
- ◆ Over 690,000 logic cells
- ◆ Gigabit Ethernet media access controllers
- ◆ On-chip 405 PowerPC RISC microcontroller cores
- ◆ Memory densities approaching 85 million bits
- ◆ Reduced power with core voltages at 1 volt
- ◆ Silicon geometries to 28 nanometers
- ◆ High-density BGA and flip-chip packaging
- ◆ Over 1200 user I/O pins
- ◆ Configurable logic and I/O interface standards



Figure 23

It's virtually impossible to keep up to date on FPGA technology, since new advancements are being made every day.

The hottest features are processor cores inside the chip, computation clocks to 500 MHz and above, and lower core voltages to keep power and heat down.

Several years ago, dedicated hardware multipliers started appearing and now you'll find literally thousands of them on-chip as part of the DSP initiative launched by virtually all FPGA vendors.

High memory densities coupled with very flexible memory structures meet a wide range of data flow strategies. Logic slices with the equivalent of over ten million gates result from steadily shrinking silicon geometries.

BGA and flip-chip packages provide plenty of I/O pins to support on-board gigabit serial transceivers and other user-configurable system interfaces.

New announcements seem to be coming out every day from chip vendors like Xilinx and Altera in a never-ending game of outperforming the competition.

FPGAs: New Development Tools

- High Level Design Tools
 - Block Diagram System Generators
 - Schematic Processors
 - High-level language compilers for VHDL & Verilog
 - Advanced simulation tools for modeling speed, propagation delays, skew and board layout
 - Faster compilers and simulators save time
 - Graphically-oriented debugging tools
- IP (Intellectual Property) Cores
 - FPGA vendors offer both free and licensed cores
 - FPGA vendors promote third party core vendors
 - Wide range of IP cores available



Figure 24

To support such powerful devices, new design tools are appearing that now open up FPGAs to both hardware and software engineers. Instead of just accepting logic equations and schematics, these new tools accept entire block diagrams as well as VHDL and Verilog definitions.

Choosing the best FPGA vendor often hinges heavily on the quality of the design tools available to support the parts.

Excellent simulation and modeling tools help to quickly analyze worst case propagation delays and suggest alternate routing strategies to minimize them within the part. This minimizes some of the tricky timing work for hardware engineers and can save one hours of tedious troubleshooting during design verification and production testing.

In the last few years, a new industry of third party IP (Intellectual Property) core vendors now offer thousands of application-specific algorithms. These are ready to drop into the FPGA design process to help beat the time-to-market crunch and to minimize risk.

FPGA Resources

FPGAs for SDR

- Parallel Processing
- Hardware Multipliers for DSP
 - FPGAs can now have over 500 hardware multipliers
- Flexible Memory Structures
 - Dual port RAM, FIFOs, shift registers, look up tables, etc.
- Parallel and Pipelined Data Flow
 - Systolic simultaneous data movement
- Flexible I/O
 - Supports a variety of devices, buses and interface standards
- High Speed
- Available IP cores optimized for special functions



Figure 25

Like ASICs, all the logic elements in FPGAs can execute in parallel. This includes the hardware multipliers, and you can now get over 3500 of them on a single FPGA.

This is in sharp contrast to programmable DSPs, which normally have just a handful of multipliers that must be operated sequentially.

FPGA memory can now be configured with the design tool to implement just the right structure for tasks that include dual port RAM, FIFOs, shift registers and other popular memory types.

These memories can be distributed along the signal path or interspersed with the multipliers and math blocks, so that the whole signal processing task operates in parallel in a systolic pipelined fashion.

Again, this is dramatically different from sequential execution and data fetches from external memory as in a programmable DSP.

As we said, FPGAs now have specialized serial and parallel interfaces to match requirements for high-speed peripherals and buses.

FPGAs Bridge the SDR Application Space

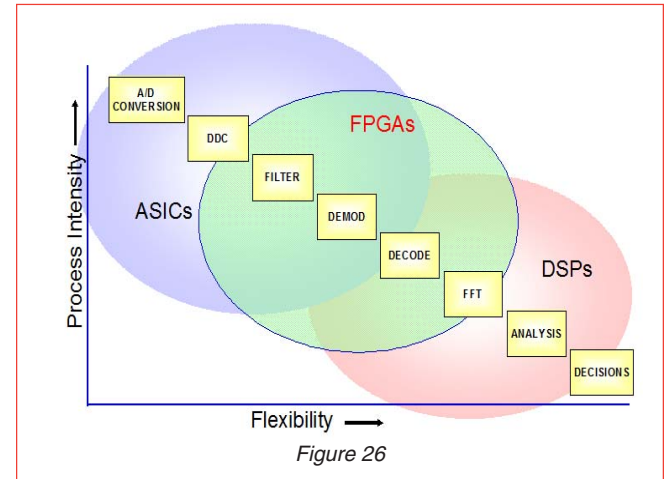


Figure 26

As a result, FPGAs have significantly invaded the application task space as shown by the center bubble in the task diagram above.

They offer the advantages of parallel hardware to handle some of the high process-intensity functions like DDCs and the benefit of programmability to accommodate some of the decoding and analysis functions of DSPs.

These advantages may come at the expense of increased power dissipation and increased product costs. However, these considerations are often secondary to the performance and capabilities of these remarkable devices.

FPGA Resources

Pentek Products with Factory-Installed SDR IP Cores

Model	Input Channels	Sampling Freq (max)	Input Bits	DDC Chan.	Decimation Range	Output Bits	DUC Chan.	Interpol. Range	Chan. Out	Out Bits	Beam-former
71621	3	200 MHz	16	3	2–64K	16 or 24	1	2–512K	2	16	Yes
71721	3	200 MHz	16	3	2–64K	16 or 24	1	2–512K	2	16	Yes
71131	8	250 MHz	16	8	2–32K	–	None	None	None	–	No
71821	3	200 MHz	16	3	2–32K	16 or 24	2	2–262K	2	16	No
71624*	2	200 MHz	16	34	512–8192	16	34	512–8192	2	–	No
71641	1 or 2	3.6 or 1.8 GHz	12	1 or 2	4, 8 or 16	16	None	None	None	–	No
71741	1 or 2	3.6 or 1.8 GHz	12	1 or 2	4, 8 or 16	16	None	None	None	–	No
71841	1 or 2	3.6 or 1.8 GHz	12	1 or 2	4, 8 or 16	16	None	None	None	–	No
71651	2	500/400 MHz	12/14	2	2–128K	16 or 24	1	2–512K	2	16	Yes
71751	2	500/400 MHz	12/14	2	2–128K	16 or 24	1	2–512K	2	16	Yes
71851	2	500/400 MHz	12/14	2	2–128K	16 or 24	1	2–512K	2	16	Yes
71661	4	200 MHz	16	4	2–64K	16 or 24	None	None	None	–	Yes
71861	4	200 MHz	16	4	2–32K	16 or 24	None	None	None	–	Yes
71662	4	200 MHz	16	32	16–8K	24	None	None	None	–	No
71663	4	200 MHz	16	1100	–	–	None	None	None	–	No
71664**	4	200 MHz	16	4	2–64K	16 or 24	None	None	None	–	Yes
71671	None	None	–	None	–	–	4	2–1024K	4	16	No
71771	None	None	–	None	–	–	4	2–1024K	4	16	No

Notes: Products use Virtex-6 FPGAs except: 71721, 71741, 71751, and 71771 which use Virtex-7 FPGAs

* Adaptive relay performance

71131, 71821, 71841, 71851, and 71861 which use Kintex FPGAs

** Meets VITA 49.0 specification

Figure 27

The above chart shows the salient characteristics for Pentek's SDR products with factory-installed IP cores. All of these products are available off-the-shelf and are in the Pentek datasheets and catalogs. The chart provides information regarding the number of input channels, maximum sampling frequency of their A/Ds, and the number of bits. This information is followed by DDC characteristics such as number of DDC channels and the decimation range.

Other information that's specific to each core is included as well as an indication of the models that include a DUC, an interpolation filter and output D/A. As shown in the chart, many of these models include features that are critical for beamforming and direction-finding applications. All the models shown are XMC modules. As with all Pentek SDR products, these models are also available in PCI Express, VPX, AMC, and CompactPCI formats.

[Click Here for the PRODUCT SELECTOR](#)

FPGA Resources

FPGA Resource Comparison

	Virtex-5 LX, SX	Virtex-6 LX, SX	Virtex-7 VX	Kintex KU035, 60, 115
Logic Cells	52K–155K	128K–314K	326K–693K	444K–1,451K
CLB Flip-Flops	32K–96K	160K–392K	408K–864K	406K–1,326K
Slices*	8K–24K	20K–49K	51K–108K	69K–207K
Block RAM (kb)	4,752–8,784	9,504–25,344	27,000–52,920	19,000–75,900
DSP Slices	128–640	480–1,344	1,120–3,600	1,700–5,520
Serial Gbit Transceivers	12–16	20–24	28–80	16–64
PCI Express Support	N/A	Gen 2 x8	Gen 2 x8, Gen3 x8	Gen 2 x8, Gen3 x8
Max. User I/O	480–680	600–720	700–1,000	416–676

*Virtex-5, Virtex-6, Virtex-7 and Kintex Slices actually represent 6.4 Logic Cells

Figure 28

The above chart compares the available resources in the four Xilinx FPGA families that are used or have been used in most of Pentek products.

- Virtex-5: LX and SX
- Virtex-6: LX and SX
- Virtex-7: VX
- Kintex UltraScale: KU035, KU060, KU115

The Virtex-5 family LX devices offer maximum logic resources, gigabit serial transceivers, and Ethernet media access controllers. The SX devices push DSP capabilities with all of the same extras as the LX.

The Virtex-5 devices offer lower power dissipation, faster clock speeds and enhanced logic slices. They also improve the clocking features to handle faster memory and gigabit interfaces. They support faster single-ended and differential parallel I/O buses to handle faster peripheral devices.

The Virtex-6 and Virtex-7 devices offer still higher density, more processing power, lower power consumption, and updated interface features to match the latest

technology I/O requirements including PCI Express. Virtex-6 supports PCIe 2.0 and Virtex-7 supports PCIe 3.0

The ample DSP slices are responsible for the majority of the processing power of the Virtex-6 and Virtex-7 families. Increases in operating speed from 550 MHz in V-5 to 600 MHz in V-6, to 900 MHz in V-7 and continuously increasing density allow more DSP slices to be included in the same-size package. As shown in the chart, Virtex-6 tops out at an impressive 1,344 DSP slices, while Virtex-7 tops out at an even more impressive 3,600 DSP slices.

The Kintex UltraScale devices offer even more performance than the Virtex-6 and Virtex-7 with less power dissipation.

The Kintex series offer PCIe Gen 2 and Gen 3 and provide a peak speed of 8 GB/sec. Pentek offers the KU035 as standard with the Kintex-based Jade products, while the KU060 and KU115 are offered as optional. The KU115 offers 5,520 DSP slices that should be enough to satisfy just about any signal-processing requirement.

Optical Resources

Optical Links Offer Many Benefits

Property	Copper	Optical
Interface Transceiver Cost	Low	High but dropping
PC Network Interface Cards	Integrated in PC or laptop	Usually optional at \$100-\$200
Power over Ethernet	Supported at low cost	Not possible
Data Rate	1 GHz	>10 GHz
Cable Loss - 100 meters	94%	3%
Max Transmission Distance	100 m (cat 6)	300 m (multi-mode) 10 km (single mode)
EMI Susceptibility Risk	Moderate	Zero
EMI Radiation Risk	Moderate	Zero
Security / Eavesdropping Risk	High	Extremely Low
Termination Costs	Low	High
Cable Cost per Length	High	Low
Cable Weight per 1000 m	60 to 600 kg	6 kg
Fire Hazard	Supports current flow if shorted	Zero
Tensile Strength	25 pounds	100-250 pounds
Cleaning Requirements	No	Yes

Figure 29

One major shortcoming of copper cable is signal loss, which becomes a serious limitation for higher frequency signals and longer cable lengths. Across a span of 100 meters, optical cables can sustain data rates up to 100 times higher than copper cable.

Because copper cables radiate electromagnetic energy, eavesdropping on network cables is a major security concern, not only for military and government customers, but also for corporations, banks, and financial institutions. Advanced signal sniffers in vehicles and briefcases are hard to detect and restrict. Optical cables are extremely difficult to “tap” without damaging the cable, resulting in immediate detection.

Signals flowing in copper cables are also susceptible to contamination from nearby sources of electromagnetic radiation, such as antennas, generators, and motors. This is critical for military and commercial aircraft and ships, as well as manned or unmanned vehicles, which are often packed with dozens of different electronic payloads. Optical cables are completely immune to EMI.

Physically, optical cables are much smaller and lighter than copper cables, especially important for weight-sensitive applications such as weapons, unmanned vehicles, and aircraft. Optical cables will operate just as well when submerged in seawater, and are completely immune to electrical shorting, especially important where explosive vapors may be present. To ease installation through conduits and passages, optical cables have smaller diameters and can withstand up to ten times more pulling tension than copper cables.

Driven by huge commercial markets for data servers, storage networks, telecom systems, and home or office internet and entertainment systems, optical interfaces are replacing older copper connections for good reasons: cost and performance. As the use of optical cables becomes more widespread, the cost per length can be much lower than copper cables that depend on commodity metal pricing. As is often the case, industrial, military and government embedded systems are now taking advantage of the many benefits of this rapidly advancing commercial technology.

Optical Resources

Optical Cables

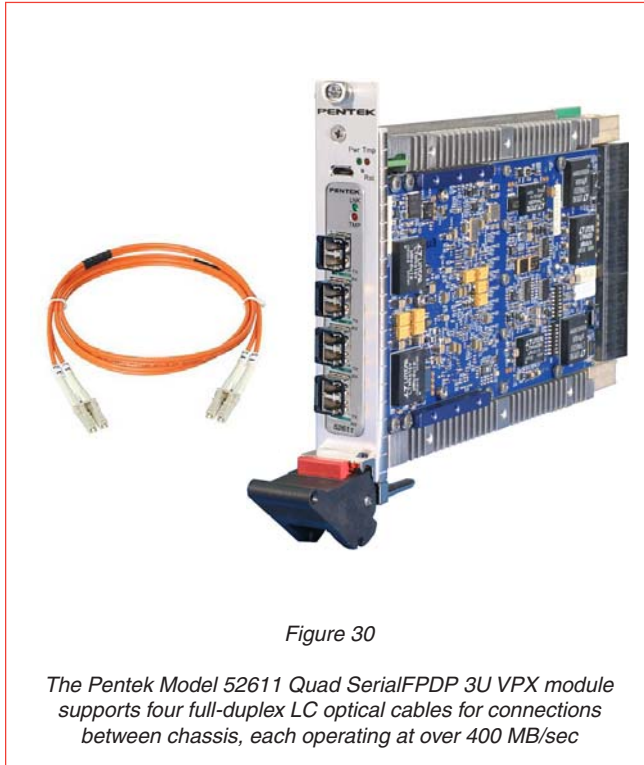


Figure 30

The Pentek Model 52611 Quad SerialFPDP 3U VPX module supports four full-duplex LC optical cables for connections between chassis, each operating at over 400 MB/sec

An optical cable is a waveguide for propagating light through an optical fibre. It consists of a central core clad with a dielectric material having a higher index of refraction than the core to ensure total internal reflection. Optical cables use either multi-mode or single-mode transmission.

Multi-mode cables accept light rays entering the core within a certain angle of the axis. They travel down the cable by repeatedly reflecting off the dielectric boundary between the core and the cladding. The core diameters are typically 50 or 62.5 μm , and the wavelength of light is typically 850 nm.

Single-mode cables propagate light as an electromagnetic wave operating in a single transverse mode straight down the fibre using typical wavelengths of 1310 and 1550 nm. The core diameter must be no greater than ten times the light wavelength, typically 8 to 10 μm . Although single-mode cables can carry signals over lengths 10 to 100 times longer than multi-mode, the transceivers are more expensive.

Hundreds of different types of optical cable connectors exist in the market, each addressing specific applications and environments. The challenge is connecting the ends of two optical cables to retain the maximum fidelity of the light interface, in spite of human factors, tolerances, contamination, and environments. Special tools and kits for cleaning the ends of each optical fibre are essential for reliable operation.

Optical Transceivers

Coupling electrical signals to light signals for transmission through optical cables requires optical transceivers. Most systems require full-duplex operation for each optical link to support flow-control and error correction. A pair of optical fibers, often bonded together in the same cable, supports transmit and receive data flowing in opposite directions.

Although several analog light modulation schemes (including AM and FM) have been used in the past, now almost all transceivers use digital modulation. Optical emitters simply translate the digital logic levels into on/off modulation of the laser light beam, while the detectors convert the modulated light back into digital signals. This physical layer interface for transporting 0s and 1s is capable of supporting any protocol.

The latest transceivers use laser emitters to support data rates to 100 Gbits/sec and higher, and each generation steadily reduces the power, size and cost of devices. Different technologies are required for emitters and detectors, but both are often combined in a single product to provide full-duplex operation.

Optical transceivers thus provide a physical layer interface between optical cables and the vast array of electrical multi-gigabit serial ports found on processors, FPGAs, and network adapters. As a result, optical transceivers are transparent to the protocols they support, making them appropriate for any high-speed serial digital link.

Electrical signals of the optical transceivers connect to the end point device, which must then handle clock encoding and recovery, synchronization, and line balance at the physical layer. Data link layer circuitry establishes framing so that data words can be sent and received across the channel.

Optical Resources

Choosing the Right Optical Protocol

Protocols define the rules and features supported by each type of system link, ranging from simple transmission of raw data to sophisticated multi-processor support for distributed networks, intelligent routing, and robust error correction. Of course, heavier protocols invariably mean less efficient data transfers and increased latency. Generally, it is best to use the simplest protocol that satisfies the system requirements.

As an example of a lightweight protocol, Aurora for Xilinx FPGAs features on-board link-layer engines and high-speed serial transceivers. Aurora is intended primarily for point-to-point connectivity for sending data between two FPGAs. It includes 8b/10b or 64b/66b channel coding to balance the transmission channel, and supports single- or full-duplex operation. Aurora handles virtually any word length and allows multiple serial lanes to be bonded into a single logical channel, aggregating single lane bit rates for higher data throughput. Data rates for each serial lane can be 12.5 Gbits/sec or higher. Extremely simple and with minimal overhead, Aurora is very efficient in linking data streams between multiple FPGAs within a module, or between modules across a backplane.

Stepping up in complexity is the SerialFPDP protocol defined under VITA 17.1. It addresses several important needs of embedded systems including flow control to avoid data overruns, and copy mode to allow one node to receive data and also forward it on to another node. The copy/loop mode supports a ring of multiple nodes eventually completing a closed loop. The nominal data rate on each lane is 2.5 Gbits/sec, but advances in device technology now support rates over twice that speed.

Infiniband defines a flexible, low-latency, point-to-point interconnect fabric for data storage and servers with current rates of 14 Gbits/sec, moving up to 50 Gbits/sec in the next few years. Channel speeds can be boosted by forming logical channels by bonding 4 or 12 lanes.

The venerable Ethernet protocol still dominates computer networks, with 10GbE now commonly supported by a vast range of computers, switches, and adapters. Even though Ethernet suffers from high overhead, making it somewhat cumbersome for high-data rate low-latency applications, its ubiquitous presence virtually assures compatibility.

VITA 49.0: VITA Radio Transport (VRT) Standard

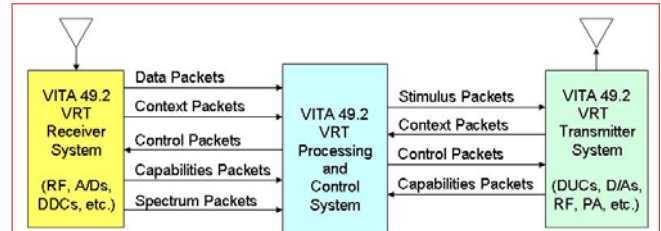


Figure 31

New extensions to the VITA VRT Protocol define standardized packets for control and status of radio receiver and transmitter equipment and digitized receive and transmit signal payload packets for added flexibility

Approved as an ANSI standard in 2007, VITA 49.0 defines standardized packets for connecting software radio systems for communications, radar, telemetry, direction finding, and other applications. The original specification addressed only receiver functions. Receive signal data packets deliver digitized payload data, a precise time stamp, and identifiers for each channel and signal. Context packets include operating parameters of the receiver including tuning frequency, bandwidth, sampling rate, gain, antenna orientation, speed, heading, etc. One notable shortcoming of the original specification was its inability to control the receiver.

VITA 49.2, a new extension to VRT now in balloting, adds control packets for delivering operational parameters to all aspects of the radio equipment, as well as support for transmitters. The new stimulus packets contain streaming digital samples of signals to be transmitted. Other new packets, called capabilities packets, inform the host control system of the available hardware in the radio along with the allowed range of parameters for control. Lastly, spectrum packets from the receiver deliver spectral information to help simplify spectral survey and energy detection operations required by the control system.

With this latest extension, VRT provides a standardized protocol for controlling and configuring all aspects of a software-radio transceiver. One major objective is enabling a common radio hardware platform to handle a wide range of applications simply by implementing new host software algorithms that exploit VRT protocols to achieve the required modes of operation.

Optical Resources

Optical Interfaces for VPX

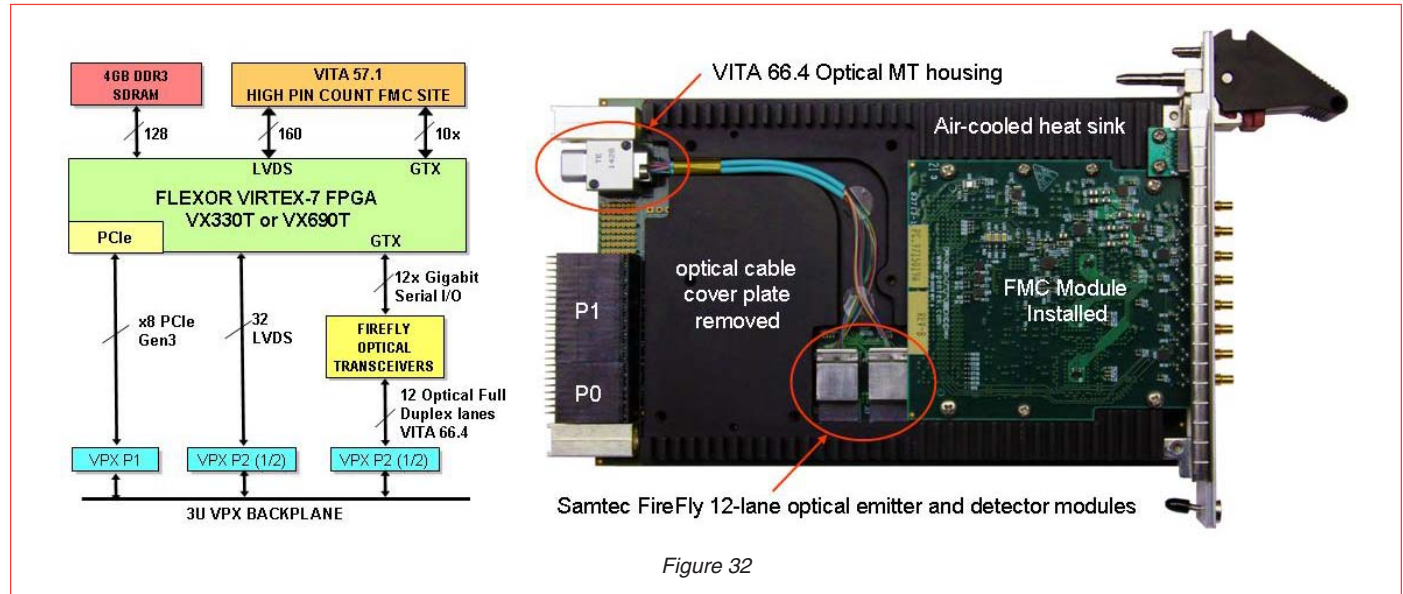


Figure 32

Although optical interfaces using various connectors and cable types have been deployed in embedded systems for years, most of them use front panel connections. This can be a maintenance issue and is often not permitted in conduction-cooled systems.

The VITA 66 Fiber Optic Interconnect group has developed a set of standards that bridge optical connections directly through the VPX backplane connector. The first three are variants for 3U and 6U systems and are based on MT, ARINC 801 Termini, and Mini-Expanded Beam optical connector technology, respectively.

The metal housings are physically dimensioned to replace one or more of the standard MultiGig RT-2 VPX bladed copper connectors. The high-density MT variant defined in VITA 66.1 provides the highest density of the three, with up to 12 or 24 pairs of optical fibers, while VITA 66.2 and 66.3 each provide 2 pairs.

A fourth standard soon to be released, VITA 66.4, uses the MT ferrule but with a metal housing half the size of VITA 66.1, thus occupying only half of the 3U VPX P2 connector position.

To simplify implementation, Samtec offers its FireFly™ Micro Fly-Over system. It consists of 12 pairs of optical fibers installed in an MT ferrule. One 12-lane optical flat

cable connects to a small VCSEL laser emitter module and the other connects to a detector module.

Figure 32 shows the industry's first implementation of the emerging VITA 66.4 standard, the Pentek Model 5973 3U VPX Virtex-7 FMC carrier. Here the electrical interfaces of the FireFly emitter and detector modules are connected directly to the GTX serial transceiver pins of the Virtex-7 FPGA. Today, FireFly transceivers are rated for 14 Gbits/sec with 28 Gbits/sec versions coming soon. With the 5973 operating at nominal data rates of 10 Gbits/sec through each optical fibre using Aurora protocol, the backplane throughput is 12 GB/sec, simultaneously in both directions.

The first version of this product uses multi-mode transceivers and cable to support cable lengths of 100 meters or more. Single-mode transceivers will extend the distance to several kilometers. A wide range of MT optical cables and connector products allow board-to-board connections across the backplane, and backplane-to-chassis connections for external MTP cables to remotely located systems.

The 12 GB/sec VITA 66.4 optical interface complements the 8 GB/sec Gen 3 x8 copper PCIe interface on VPX P1, offering plenty of I/O for demanding applications. System engineers can now choose between optical and copper links to solve high-data rate connectivity requirements.

Products

PMC, XMC, PCI Express, OpenVPX, AMC, FMC, and CompactPCI Software Radio and Supporting Products

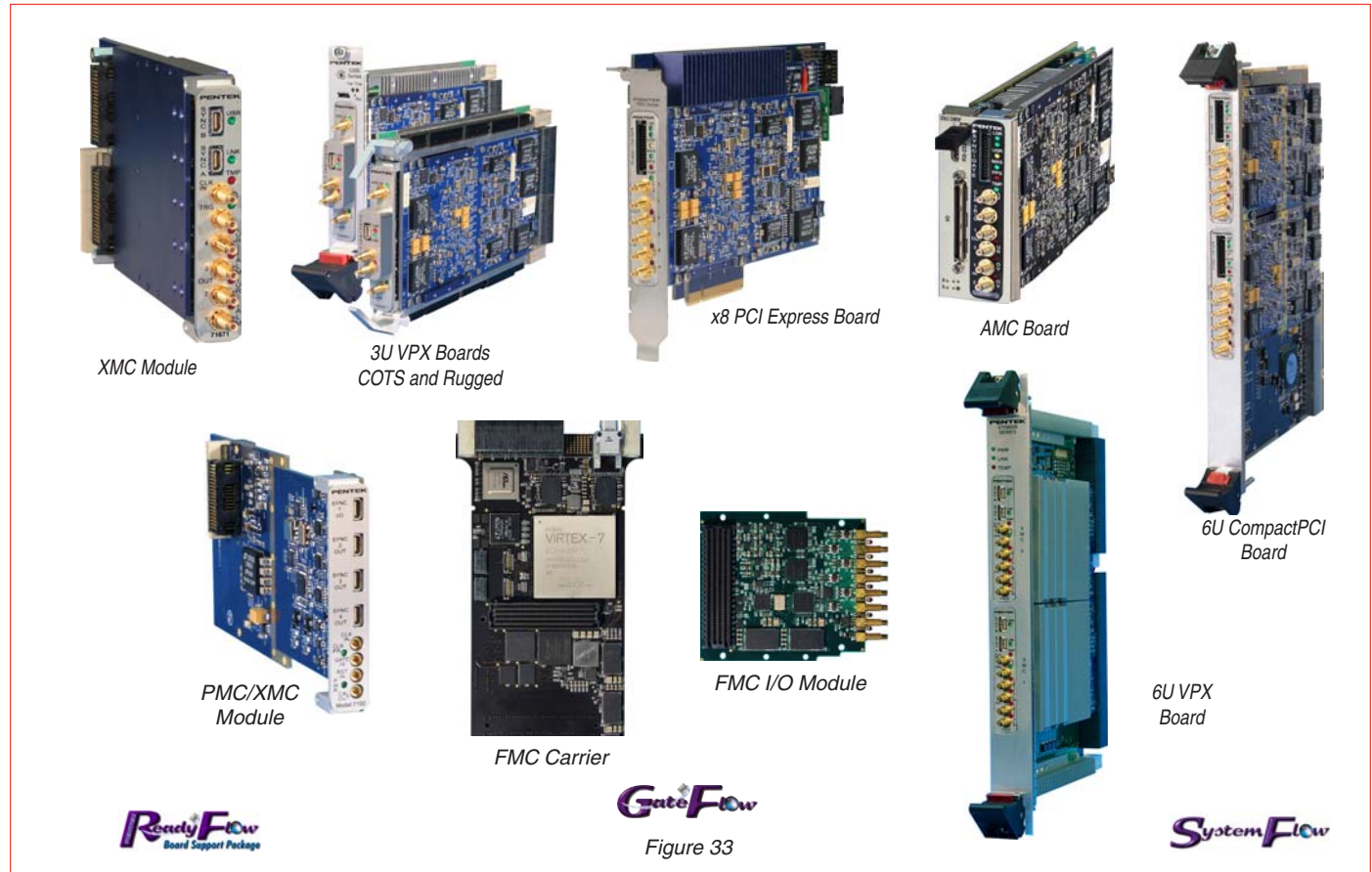


Figure 33

The Pentek family of board-level software radio products is the most comprehensive in the industry. All of these products are available in several formats to satisfy a wide range of requirements: PMC/XMC, PCI Express, 3U and 6U VPX, AMC, FMC, 3U and 6U CompactPCI.

Software radio products are supported by clock synthesizer, synchronizer and distribution boards. These products are also available in the same formats as the software radio products.

In addition to their commercial versions, many of the above products are available in ruggedized versions up to and including conduction-cooled.

All Pentek software radio products include multiboard synchronization that facilitates the design of multichannel systems with synchronous clocking, gating and triggering.

Pentek's comprehensive software support includes the ReadyFlow[®] Board Support Package, the GateFlow[®] FPGA Design Kit and high-performance factory-installed IP cores that expand the features and range of many Pentek software radio products. In addition, Pentek high-speed recording systems are supported with SystemFlow[®] recording software that features a Windows[®]-based graphical user interface.

In addition to the product overviews presented in the pages that follow, active links to their datasheets and the datasheets of similar products on Pentek's website, are included with each product.

Products

Cobalt, Onyx and Jade XMC Models

Model	Cobalt	Onyx	Jade	A/D Converters		D/A Converters		IP or Other I/O Type
				#	Type	#	Type	
71x20	✓	✓	✗	3	200 MHz / 16-bit	2	800 MHz / 16-bit	
71x21	✓	✓	✓	3	200 MHz / 16-bit	2	800 MHz / 16-bit	DDC Interp Sum
71x24	✓	✗	✗	3	200 MHz / 16-bit	2	800 MHz / 16-bit	Adaptive Relay
71x60	✓	✓	✗	4	200 MHz / 16-bit			
71x61	✓	✓	✓	4	200 MHz / 16-bit			DDC Sum
71x62	✓	✓	✓	4	200 MHz / 16-bit			DDC
71x63	✓	✗	✗	4	200 MHz / 16-bit			GSM Channelizer
71x64	✓	✓	✓	4	200 MHz / 16-bit			DDC VITA-49
71x90	✓	✓	✓	2	200 MHz / 16-bit			.925 – 2.175 GHz L-Band Tuner
71x50-014	✓	✗	✗	2	400 MHz / 14-bit	2	800 MHz / 16-bit	
71x50	✓	✗	✗	2	500 MHz / 12-bit	2	800 MHz / 16-bit	
71x51-014	✓	✓	✓	2	400 MHz / 14-bit	2	800 MHz / 16-bit	DDC Interp Sum
71x51	✓	✓	✓	2	500 MHz / 12-bit	2	800 MHz / 16-bit	DDC Interp Sum
71x30	✓	✓	✓	1	1 GHz / 12-bit	1	1 GHz / 16-bit	
71x40	✓	✗	✗	1 2	3.6 GHz / 12-bit 1.8 GHz / 12-bit			
71x41	✓	✓	✓	1 2	3.6 GHz / 12-bit 1.8 GHz / 12-bit			DDC
71x70	✓	✗	✗			4	1.25 GHz / 16-bit	
71x71	✓	✓	✓			4	1.25 GHz / 16-bit	Interp
71x10	✓	✓	✓					32 pair LVDS I/O
71x11	✓	✓	✓					Quad Serial FPDP

Notes

- The chart above lists only the 71xxx XMC products that form the basis of all Cobalt, Onyx and Jade product lines.
- By changing the 2nd digit of the model number to “2”, the 72xxx 6U cPCI products offer the same resources as the table above, plus an extra available XMC site.
- By changing the 2nd digit to “3”, the 73xxx 3U cPCI products offer the same resources as the table above.
- By changing the second digit to “4” the 74xxx 6U cPCI products offer twice the resources shown in the table.
- By changing the 2nd digit to “8” the 78xxx PCIe products offer the same resources as the products in the table.
- By changing the 1st and 2nd digits to “52”, the 52xxx 3U VPX products offer the same resources as the table.
- By changing the 1st and 2nd digits to “53”, the 53xxx 3U VPX products offer a crossbar switch to the backplane.
- By changing the 1st and 2nd digits to “56”, the 56xxx AMC products offer the same resources as shown in the table.
- By changing the 1st and 2nd digits to “57”, the 57xxx 6U VPX products offer the same resources, plus an extra available XMC site.
- By changing the 1st and 2nd digits of the model number to “58”, the 58xxx 6U VPX products offer twice the resources shown in the table above.

Figure 34

Products

VPX Families for Cobalt Products

VPX Family Comparison		
	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x8
Option -104 path	20 pairs on VPX P2	
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

Figure 35-A

Pentek offers two families of Cobalt® 3U VPX products: the 52xxx and the 53xxx. For more information on a 52xxx or a 53xxx product, please refer to the product descriptions in the pages that follow. The table above provides a comparison of the main features of the families. Cobalt products utilize the Xilinx Virtex-6 FPGA.

VPX Families for Onyx Products

VPX Family Comparison		
	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPXP2	20 pairs on VPXP2
Option -105 path	Two x4 or one x8 on VPX P1	Two x4 or one x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

Figure 35-B

Pentek offers two families of Onyx® 3U VPX products: the 52xxx and the 53xxx. For more information on a 52xxx or a 53xxx product, please refer to the product descriptions in the pages that follow. The table above provides a comparison of the main features of the families. Onyx products utilize the Xilinx Virtex-7 FPGA.

3U VPX Family Comparison		
	52xxx	53xxx
Form Factor	3U VPX	
# of XMCs	One XMC	
Crossbar Switch	No	Yes
PCIe path	VPX P1	VPX P1 or P2
PCIe width	x4	x4 or x8
Option -104 path	24 pairs on VPXP2	20 pairs on VPXP2
Option -105 path	One x8 on VPX P1	One x8 on VPX P1 or P2
Lowest Power	Yes	No
Lowest Price	Yes	No

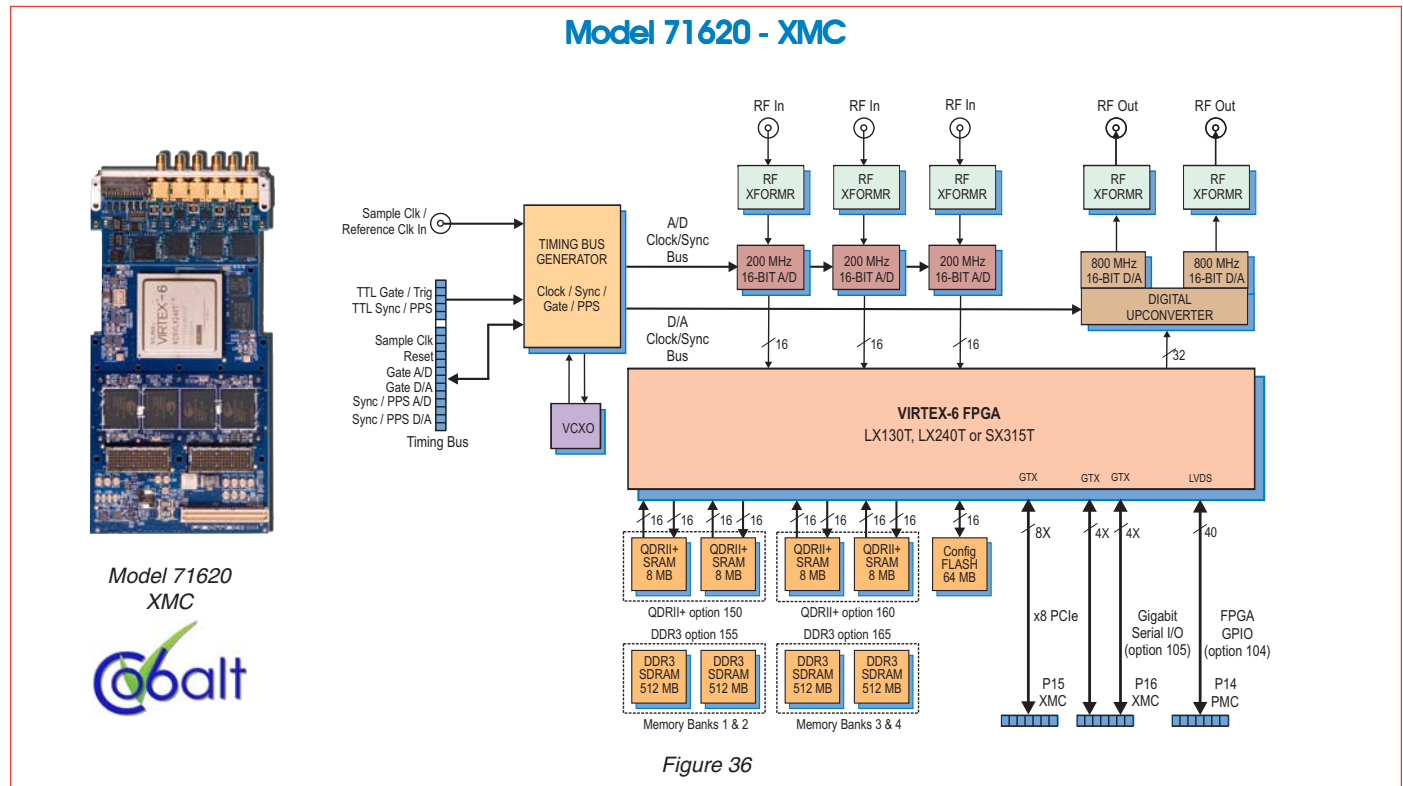
Figure 35-C

VPX Families for Jade Products

Pentek offers two families of Jade™ 3U VPX products: the 52xxx and the 53xxx. For more information on a 52xxx or a 53xxx product, please refer to the product descriptions in the pages that follow. The table above provides a comparison of the main features of the families. Jade products utilize the Xilinx Kintex UltraScale FPGA.

Products

3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA



Model 71620 is a member of the Cobalt® family of high-performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution. It includes three 200 MHz, 16-bit A/Ds, a DUC with two 800 MHz, 16-bit D/As and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71620 includes general purpose and gigabit serial connectors for application-specific I/O.

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71620 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions.

Multiple 71620's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules. The architecture supports up to four memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or combinations.

Versions of the [71620](#) are also available as an x8 PCIe half-length board (Model [78620](#)), 3U VPX (Models [52620](#) and [53620](#)), 6U VPX (Models [57620](#) and [58620](#) dual density), AMC (Model [56620](#)), 6U cPCI (Models [72620](#) and [74620](#) dual density), and 3U cPCI (Model [73620](#)).

Products

3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-7 FPGA

Model 71720 - XMC

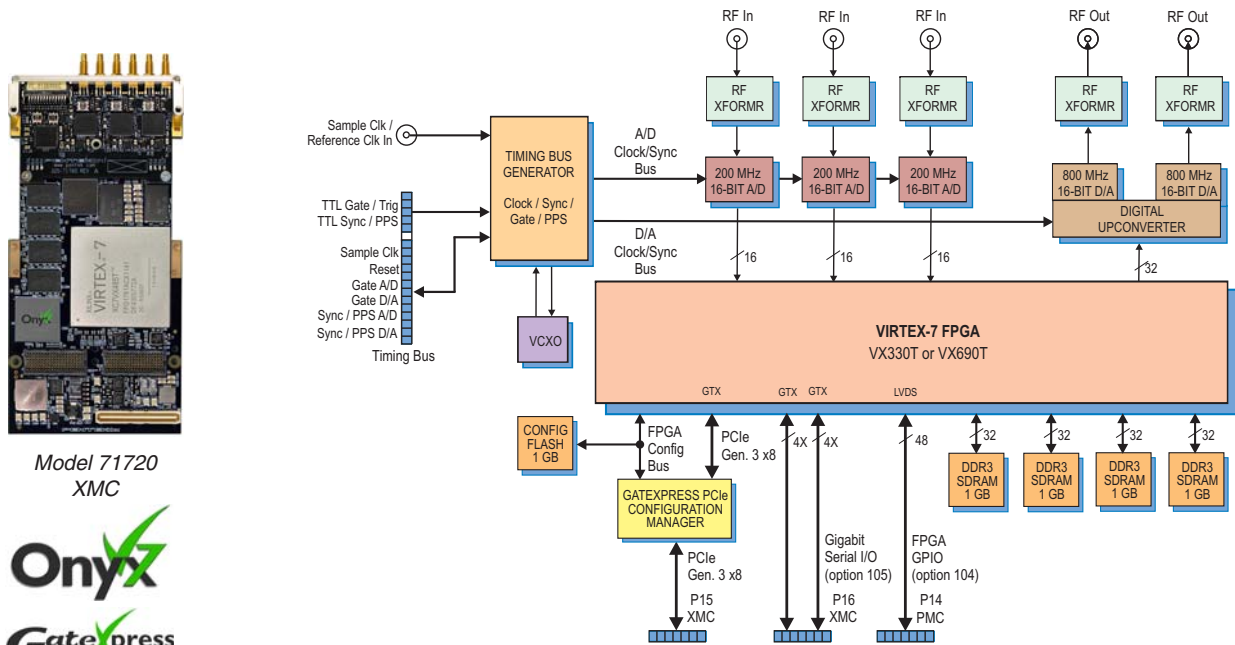


Figure 37

Model 71720 is a member of the Onyx® family of high-performance XMC modules based on the Xilinx Virtex-7 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution. It includes three 200 MHz, 16-bit A/Ds, a DUC with two 800 MHz, 16-bit D/As and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71720 includes general-purpose and gigabit-serial connectors for application-specific I/O.

The Pentek Onyx architecture features a Virtex-7 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71720 factory-installed functions include three A/D acquisition and a D/A waveform playback IP modules for simplifying data capture and data transfer. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions.

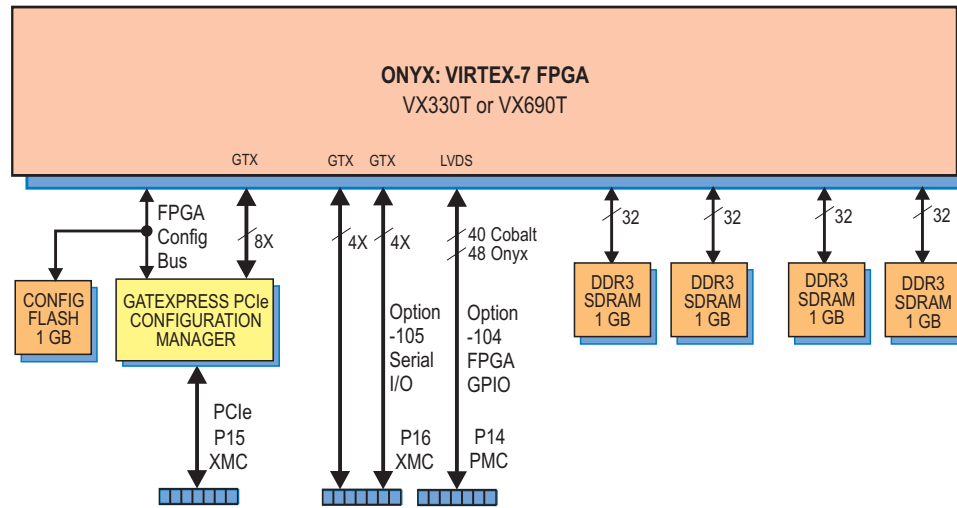
Multiple 71720's can be driven from the LVPECL bus master, supporting synchronous sampling and sync.

Versions of the [71720](#) are also available as an x8 PCIe half-length board (Model [78720](#)), 3U VPX (Models [52720](#) and [53720](#)), 6U VPX (Models [57720](#) and [58720](#) dual density), AMC (Model [56720](#)), 6U cPCI (Models [72720](#) and [74720](#) dual density), and 3U cPCI (Model [73620](#)).

GateXpress® is a sophisticated configuration manager for loading and reloading the Virtex-7 FPGA. More information is available in the next page.

Products

GateXpress for FPGA-PCIe Configuration Management



GateXpress

Onyx

Figure 38

The Onyx architecture includes GateXpress®, a sophisticated FPGA-PCIe configuration manager for loading and reloading the FPGA. At power up, GateXpress immediately presents a PCIe target for the host computer to discover, effectively giving the FPGA time to load from FLASH. This is especially important for larger FPGAs where the loading times can exceed the PCIe discovery window, typically 100 msec on most PCs.

The board's configuration FLASH can hold four FPGA images. Images can be factory-installed IP or custom IP created by the user, and programmed into the FLASH via JTAG using Xilinx iMPACT or through the board's PCIe interface. At power up the user can choose which image will load based on a hardware switch setting.

Once booted, GateXpress allows the user three options for dynamically reconfiguring the FPGA with a new IP image. The first is the option to load an alternate image from FLASH through software control. The user selects the desired image and issues a reload command.

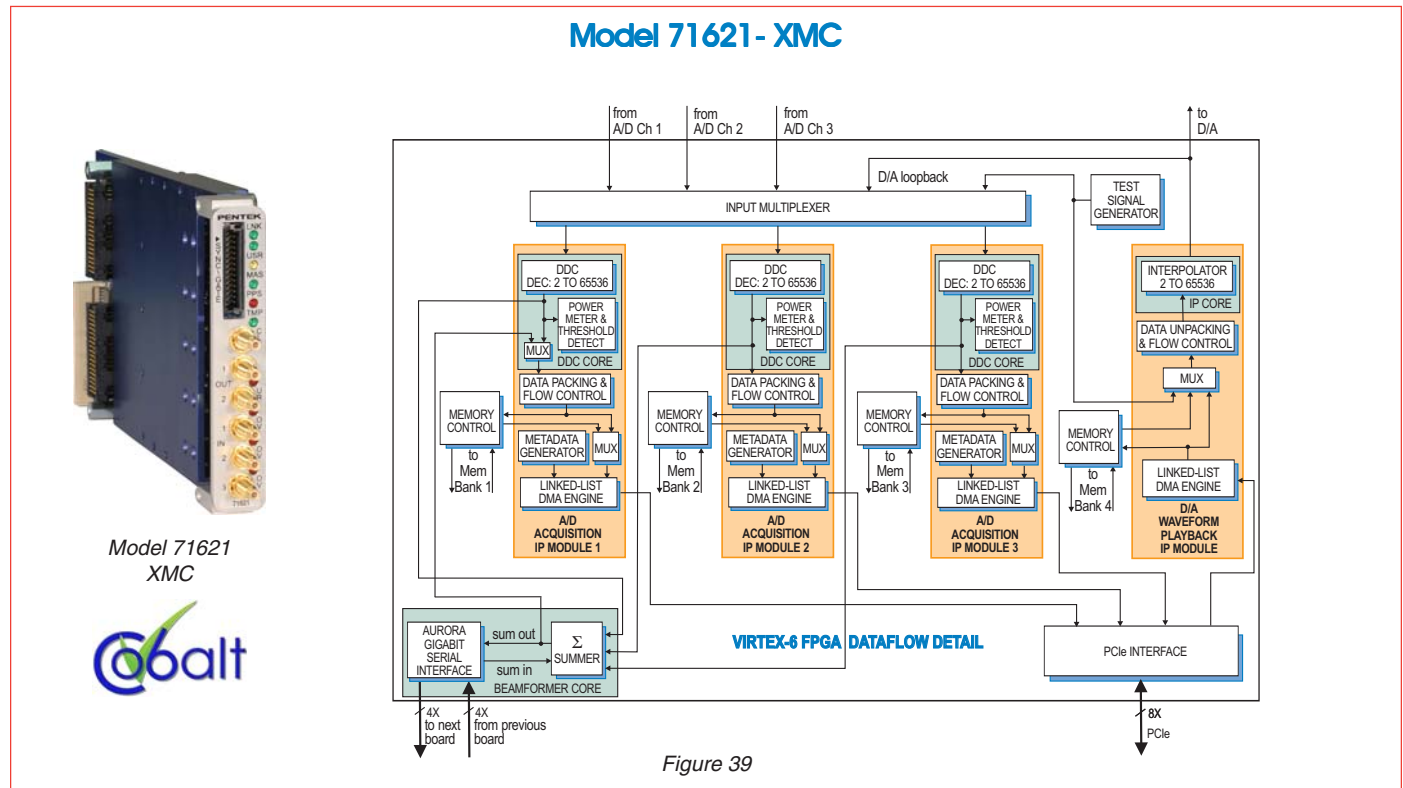
The second option is for applications where the FPGA image must be loaded directly through the PCIe interface. This is important in security situations where there can be no latent user image left in nonvolatile memory when power is removed. In applications where the FPGA IP may need to change many times during the course of a mission, images can be stored on the host computer and loaded through PCIe as needed.

The third option, typically used during development, allows the user to directly load the FPGA through JTAG using Xilinx iMPACT.

In all three FPGA loading scenarios, GateXpress handles the hardware negotiation simplifying and streamlining the loading task. In addition, GateXpress preserves the PCIe configuration space allowing dynamic FPGA reconfiguration without needing to reset the host computer to rediscover the board. After the reload, the host simply continues to see the board with the expected device ID.

Products

3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Installed IP Cores, Virtex-6 FPGA



Model 71621 is a member of the Cobalt family of high-performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter based on the Model 71620 described in the previous page, it includes factory-installed IP cores to enhance the performance of the 71620 and address the requirements of many applications.

The 71621 factory-installed functions include three A/D acquisition and one D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s , where f_s is

the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The 71621 also features a complete beamforming subsystem. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The power meters present average power measurements for each DDC core output in easy-to-read registers. A threshold detector automatically sends an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

Versions of the [71621](#) are also available as an x8 PCIe half-length board (Model [78621](#)), 3U VPX (Models [52621](#) and [53621](#)), 6U VPX (Models [57621](#) and [58621](#) dual density), AMC (Model [56621](#)), 6U cPCI (Models [72621](#) and [74621](#) dual density), and 3U cPCI (Model [73621](#)).

Products

3-Channel 200 MHz A/D, DUC, 2-Channel 800 MHz D/A, Installed IP Cores, Virtex-7 FPGA

Model 56721- AMC

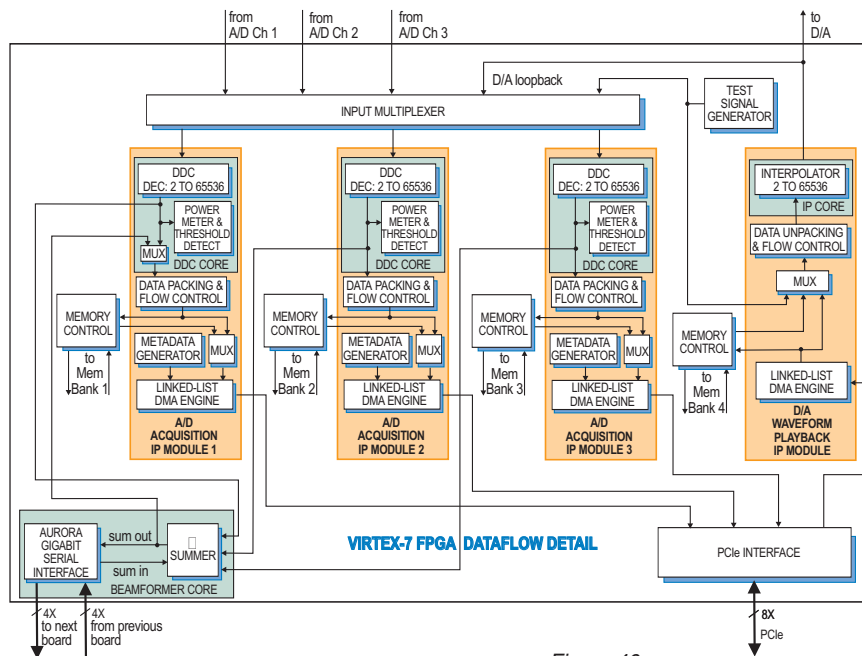


Figure 40



Model 56721
AMC



Gatepress See page 27

Model 56721 is a member of the Onyx family of high-performance AMC modules based on the Xilinx Virtex-7 FPGA. A multichannel, high-speed data converter based on the Model 71720 described previously, it includes factory-installed IP cores to enhance the performance of the 71720 and address the requirements of many applications.

The 56721 factory-installed functions include three A/D acquisition and one D/A waveform playback IP modules. Each of the three acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s , where f_s is

the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as three different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The 56721 also features a complete beamforming subsystem. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The power meters present average power measurements for each DDC core output in easy-to-read registers. A threshold detector automatically sends an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

Versions of the 56721 are also available as an XMC module (Model 71721), x8 PCIe board (Model 78721), 3U VPX (Models 52721 and 53721), 6U VPX (Models 57721 and 58721 dual density), 6U cPCI (Models 72721 and 74721 dual density), and 3U cPCI (Model 73721).

Products

3-Channel 200 MHz A/D, DDC, DUC, 2-Channel 800 MHz D/A, Installed IP Cores, Kintex UltraScale FPGA

Model 71821- XMC



Model 71821
XMC

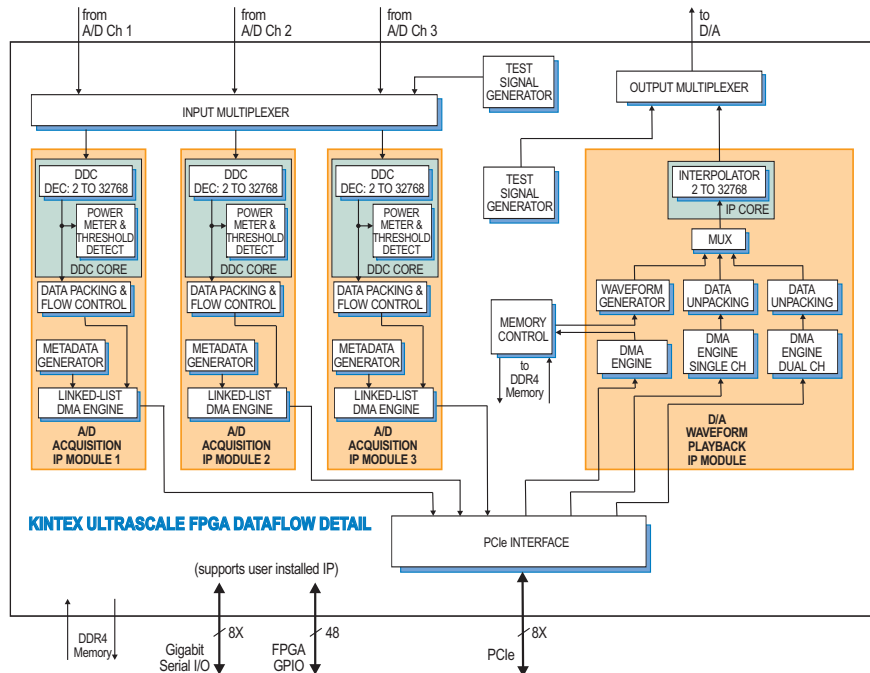


Figure 41

Model 71821 is a member of the Jade™ family of high-performance XMC modules. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 71821 is a 3-channel, high-speed data converter with programmable DDCs. It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes three A/Ds, a complete multi-board clock and sync section, a large DDR4 memory, three DDCs, one DUC and two D/As. In addition to supporting

PCI Express Gen. 3 as a native interface, the Model 71821 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The 71821 factory-installed functions include three A/D acquisition and a waveform playback IP module for simplifying data capture and playback, and data transfer between the board and a host computer. Additional IP includes: three powerful, programmable DDC IP cores; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; two test signal generators; a programmable interpolator; and a PCIe interface. These complete the factory-installed functions and enable the 71821 to operate as a complete turnkey solution for many applications.

Versions of the [71821](#) are also available as an x8 PCIe half-length board (Model [78821](#)), 3U VPX (Models [52821](#) and [53821](#)), 6U VPX (Models [57821](#) and [58821](#) dual density), AMC (Model [56821](#)), 6U cPCI (Models [72821](#) and [74821](#) dual density), and 3U cPCI (Model [73821](#)).

Products

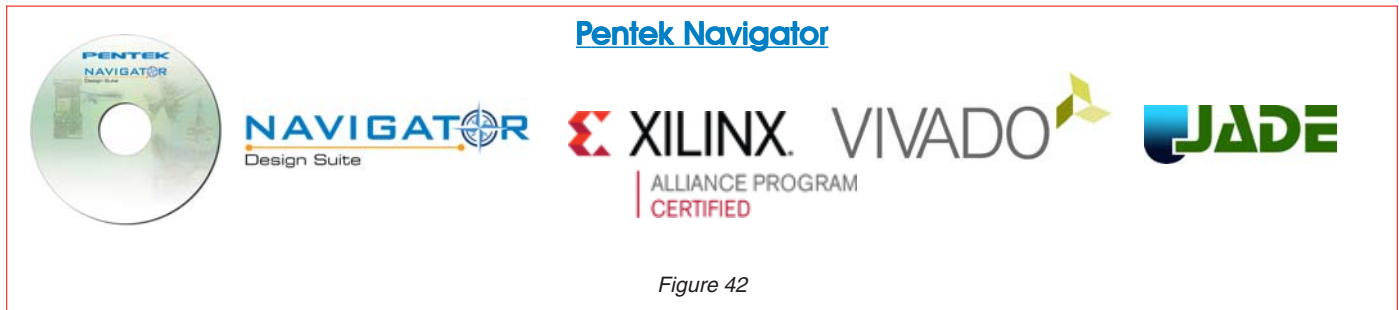


Figure 42

Pentek's Navigator Design Suite includes the Navigator FDK (FPGA Design Kit) for integrating custom IP into the Pentek factory-shipped design and the Navigator BSP (Board Support Package) for creating host applications. The Navigator Design Suite takes a new approach to solving FPGA IP and control software connectivity.

Most modern FPGA-processing applications require development of specialized FPGA IP to run on the hardware, *and* software to control the FPGA hardware from a host computer.

Even when “turnkey” solutions are delivered with complete FPGA IP and software libraries, as developers add their own custom-processing IP, new software needs to be created to control the custom IP functions.

Problems often arise when the IP and software development tools treat application development as two separate tasks. Changes to FPGA IP and control software can quickly get out of sync, complicating new application development or even breaking the formally functioning turnkey components.

The Navigator Design Suite was designed from the ground up to work with Pentek's Jade™ architecture and provide a better solution to the complex task of IP and software creation.

As FPGAs become larger and IP more complex, the need for IP design tools to manage this growing complexity has never been greater.

The Xilinx Vivado Design Suite includes IP Integrator, the industry's first plug-and-play IP integration design environment. Built around a graphical block diagram interface, IP Integrator allows IP developers to leverage existing IP by importing it into their block diagram design. Pentek's Navigator FPGA Design Kit (FDK), was designed with this exact purpose.

Each Navigator FDK provides the complete IP for a specific Jade data acquisition and processing board. When the design is opened in Vivado's IP Integrator, the developer can access every component of the Pentek design, replacing or modifying blocks as needed for the application. All blocks use industry standard AXI4 interfaces providing a well-defined format for custom IP to connect to the rest of the design. Each Navigator/Jade design includes User Blocks in the data-flow path, ideal for inserting custom processing IP.

The Navigator FDK includes complete documentation, test benches and full VHDL source for developers who desire complete access to the IP. In addition to the IP specific to the supported Jade board, Navigator also includes processing blocks for some of the most commonly used algorithms. ➤

Products

Pentek Navigator

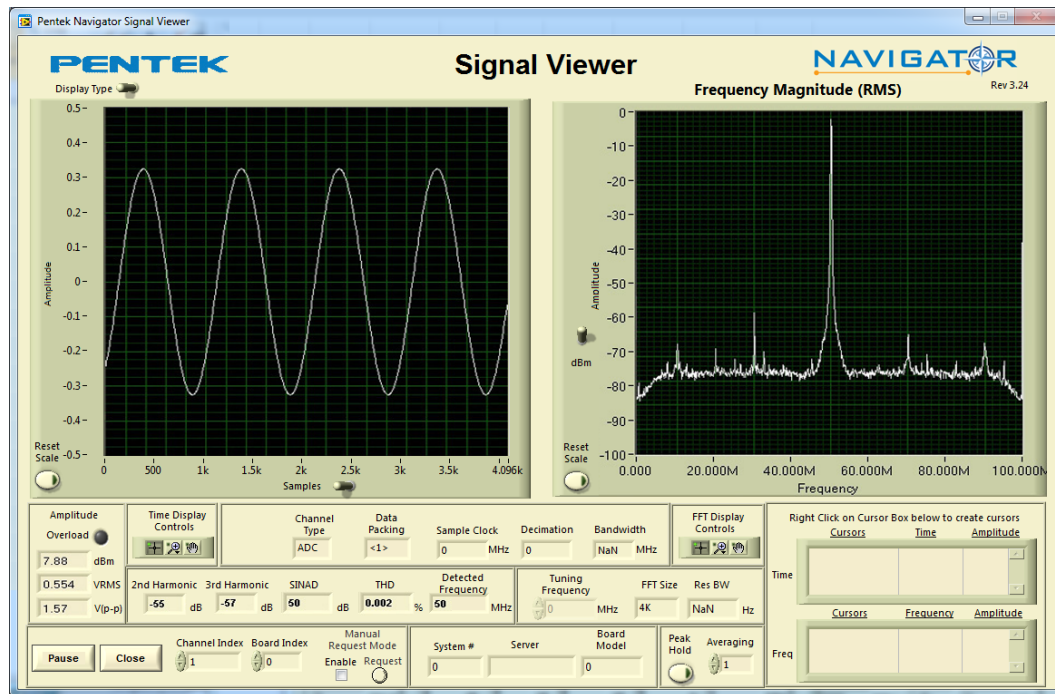


Figure 43

The companion product to the Navigator FDK is the Pentek Navigator Board Support Package (BSP). While Navigator FDK provides a streamlined path for creating or modifying new IP for the Pentek hardware, the Navigator BSP enables complete operational control of the hardware and all IP functions in the FPGA.

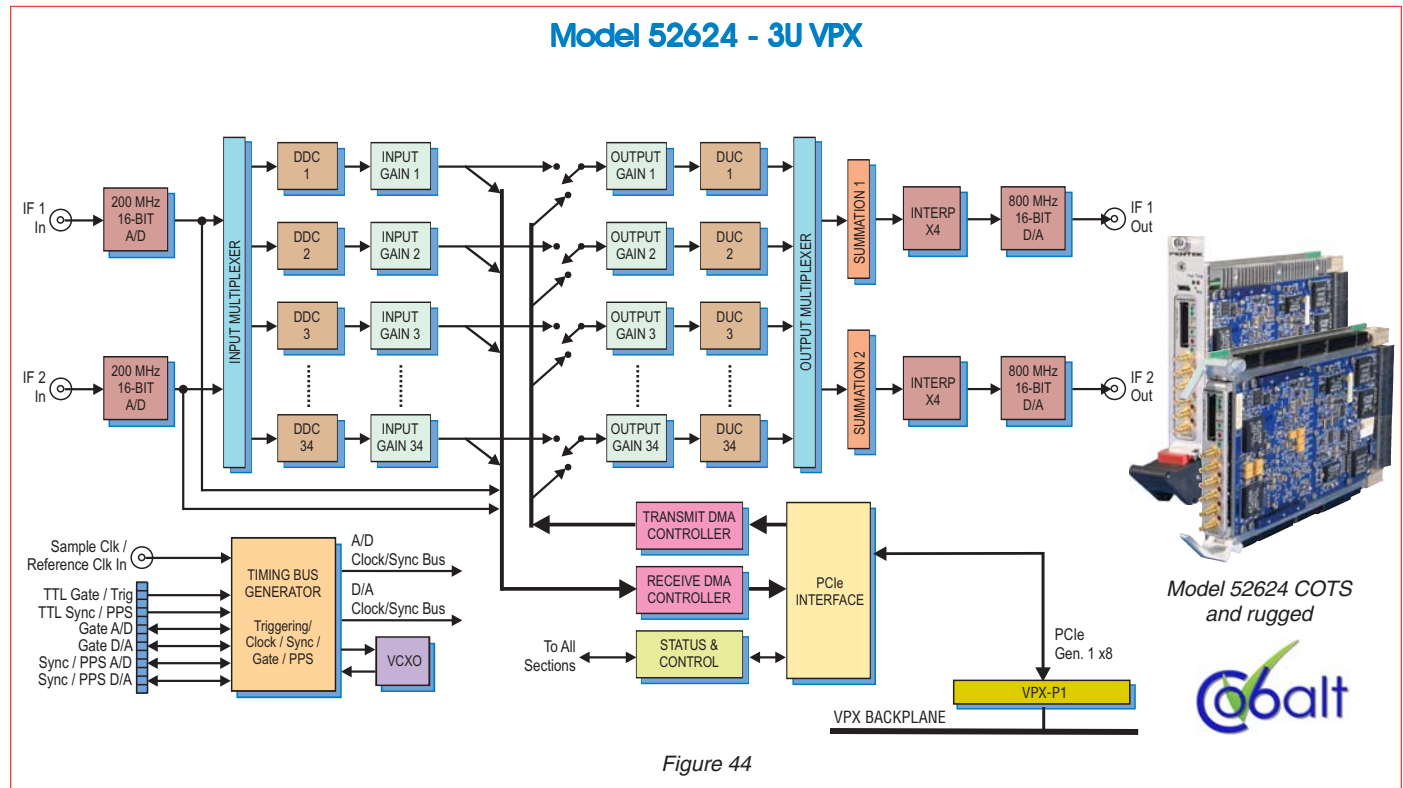
Similar to the FDK, the BSP allows software developers to work at a higher level, abstracting many of the details of the hardware through an intuitive API. The API allows developers to focus on the task of creating the application by letting the API, the hardware and IP-control libraries below it to handle many of the board-specific functions. Developers who want full access to the entire BSP library, enjoy complete C-language source code as well as full documentation.

New applications can be developed on their own or by building on one of the included example programs. All Jade boards are shipped with a full suite of build-in functions allowing operation without the need for any custom IP development. Many users find these functions ideal for addressing their application requirements.

The Navigator BSP includes the Signal Analyzer, a full-featured analysis tool, that displays data in time and frequency domains. Built-in measurement functions display 2nd and 3rd harmonics, THD (total harmonic distortion), and SINAD (signal to noise and distortion). Interactive cursors allow users to mark data points and instantly calculate amplitude and frequency of displayed signals. With the Signal Analyzer users can install the Pentek hardware and Navigator BSP and start viewing analog signals immediately.

Products

Dual-Channel 34-Signal Adaptive IF Relay, Installed IP Cores, Virtex-6 FPGA



Model 52624 is a member of the Cobalt family of high-performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. As an IF relay, it accepts two IF analog input channels, modifies up to 34 signals, and then delivers them to two analog IF outputs. Any signal within each IF band can be independently enabled or disabled, and changed in both frequency and amplitude as it passes through the board.

The 52624 supports many useful functions for both commercial and military communications systems including signal drop/add/replace, frequency shifting and hopping, amplitude equalization, and bandwidth consolidation. Applications include countermeasures, active tracking and monitoring, channel security, interception, adaptive spectral management, jamming, and encryption.

The Pentek Cobalt product family features the Virtex-6 FPGA. All of the board's data converters, interfaces and control lines are connected to the FPGA, which performs the data-routing and DSP functions for the adaptive relay.

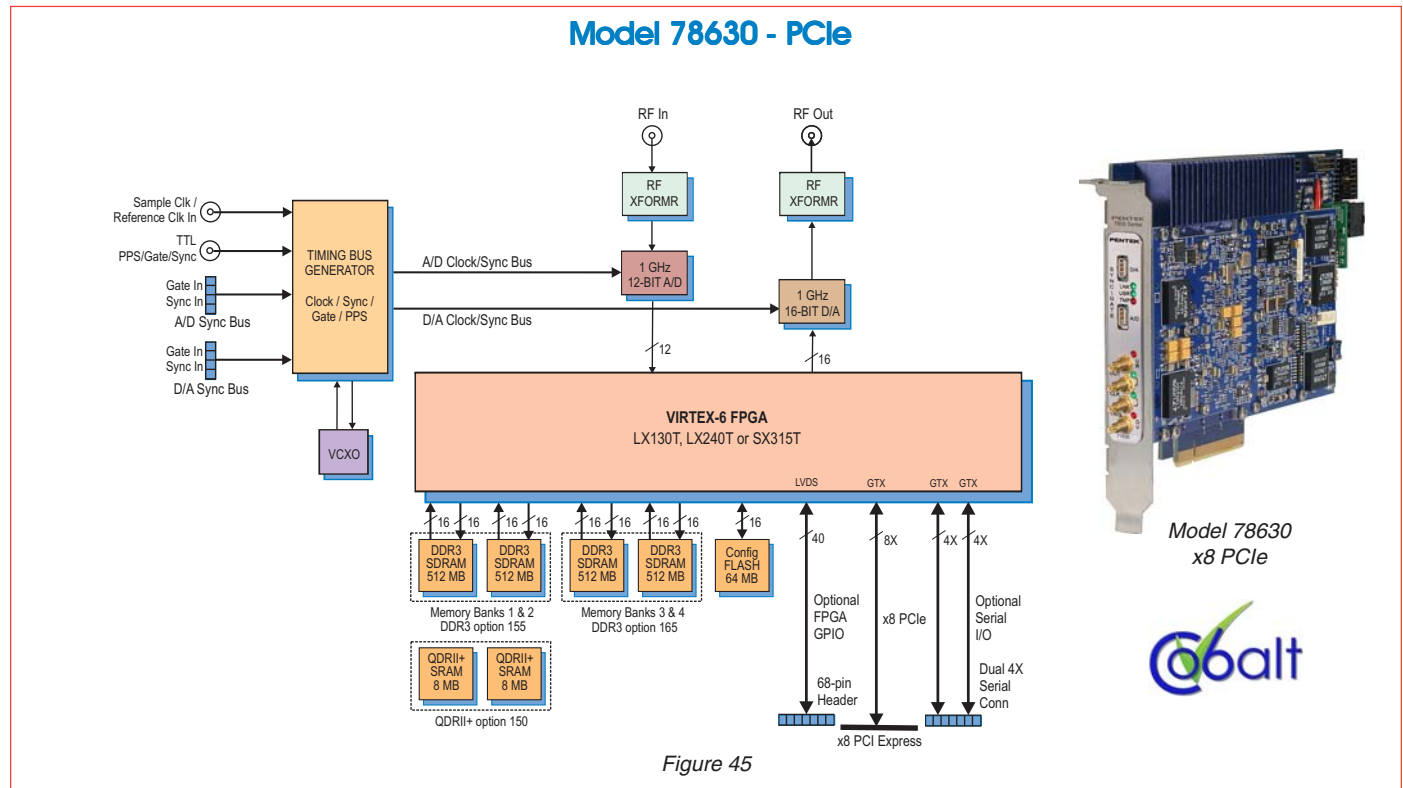
A PCIe Gen 1 system interface supports control, status and data transfers.

The Model 52624 digitizes two analog IF inputs using two 200 MHz 16-bit A/D converters. The bandwidth of each IF signal can be up to 80 MHz, and may contain multiple signals, each centered at a different frequency. An array of 34 DDCs can be independently programmed to translate any signal to baseband and then bandlimit the signal as required. DDC tuning frequency is programmable from 0 Hz to the A/D sample rate. Output bandwidth is programmable from around 20 kHz to 312 kHz for a sample rate of 200 MHz. Each DDC can independently source IF data from either of the two A/Ds.

Versions of the [52624](#) are also available as a different 3U VPX (Model [53624](#)), 6U VPX (Models [57624](#) and [58624](#) with dual density), XMC module (Model [71624](#)), an x8 PCIe board (Model [78624](#)), AMC (Model [56624](#)), 6U cPCI (Models [72624](#) and [74624](#) dual density), and 3U cPCI (Model [73624](#)).

Products

1 GHz A/D, 1 GHz D/A, Virtex-6 FPGA



Model 78630 is a member of the Cobalt family of high-performance PCIe boards based on the Xilinx Virtex-6 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. It includes 1 GHz, 12-bit A/D, 1 GHz, 16-bit D/A converters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 78630 includes optional general purpose and gigabit serial card connectors for application-specific I/O protocols.

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

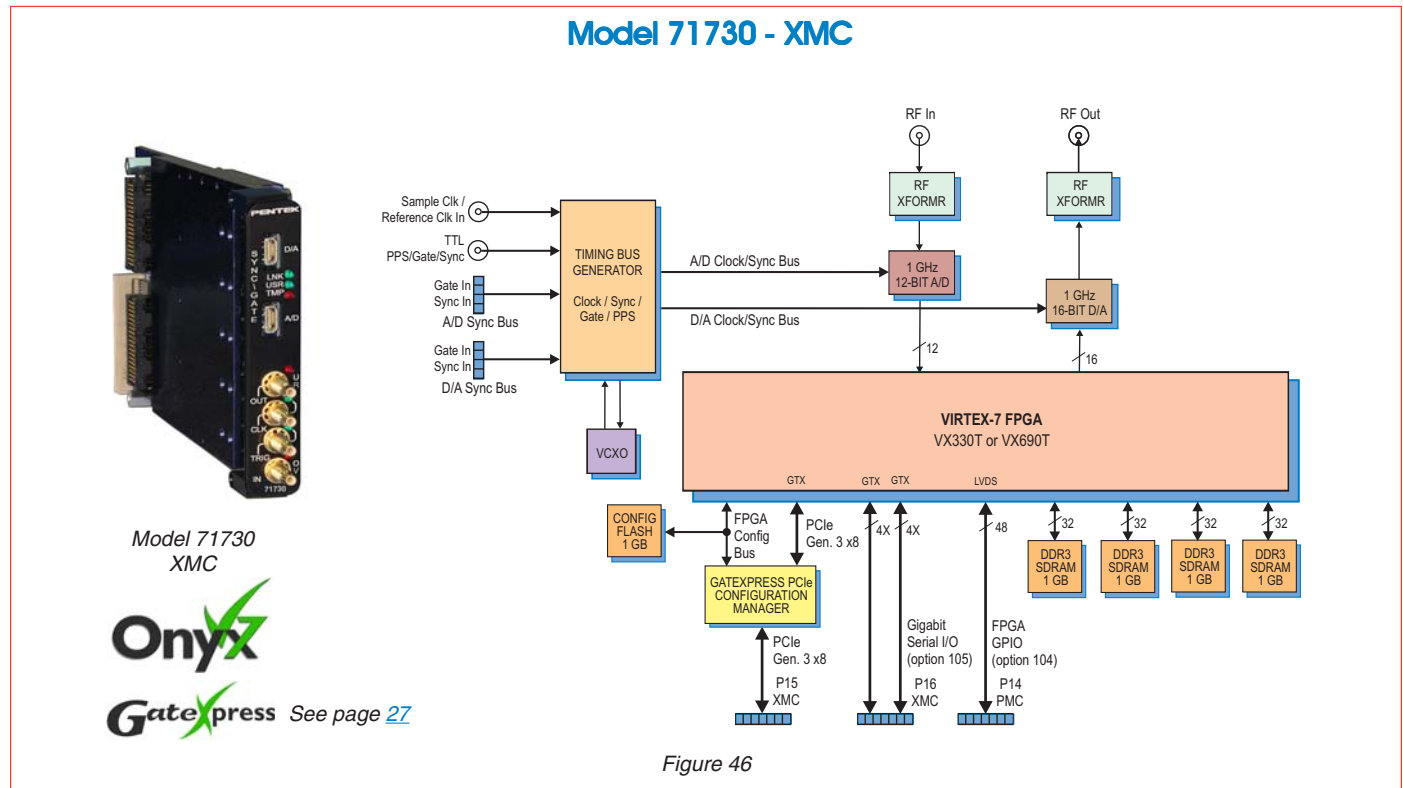
Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78630 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions.

Multiple 78630's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. The architecture supports up to four memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combinations.

Versions of the [78630](#) are also available as an XMC module (Model [71630](#)), 3U VPX (Models [52630](#) and [53630](#)), 6U VPX (Models [57630](#) and [58630](#) with dual density), AMC (Model [56630](#)), 6U cPCI (Models [72630](#) and [74630](#) with dual density), and 3U cPCI (Model [73630](#)).

Products

1 GHz A/D, 1 GHz D/A, Virtex-7 FPGA



Model 71730 is a member of the Onyx family of high-performance XMC modules based on the Xilinx Virtex-7 FPGA. A high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. It includes 1 GHz A/D and D/A converters and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71730 includes optional general purpose and gigabit serial card connectors for application-specific I/O.

The Pentek Onyx architecture features a Virtex-7 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

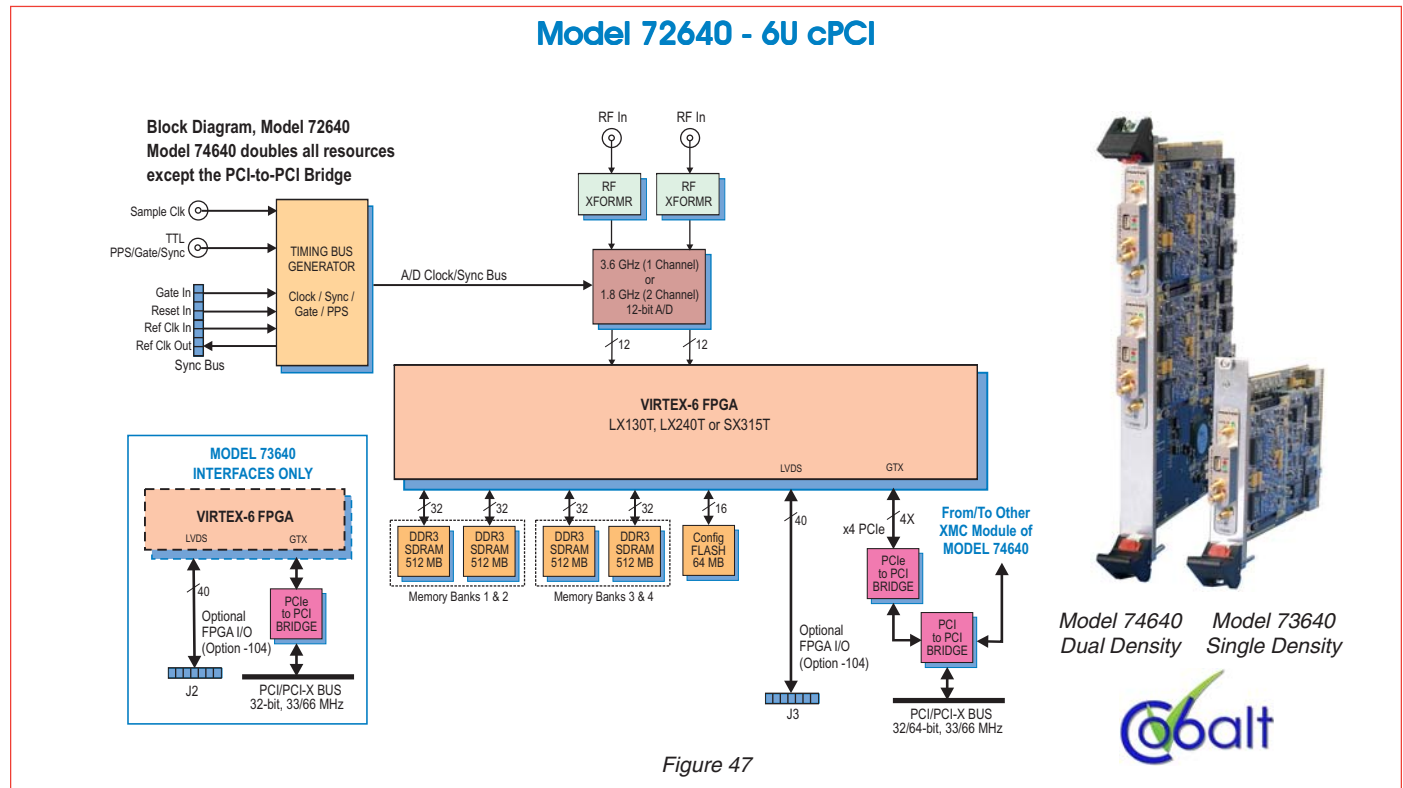
Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71730 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module for simplifying data capture and data transfer. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 71730 to operate without the need to develop any FPGA IP.

The front end accepts an analog HF or IF input on a front panel SSMC connector with transformer coupling into a TI ADS5400 1 GHz, 12-bit A/D converter. The digital outputs are delivered to the Virtex-7 FPGA for signal processing, etc.

Versions of the [71730](#) are also available as an x8 PCIe half-length board (Model [78730](#)), 3U VPX (Models [52730](#) and [53730](#)), 6U VPX (Models [57730](#) and [58730](#) dual density), AMC (Model [56730](#)), 6U cPCI (Models [72730](#) and [74730](#) with dual density), and 3U cPCI (Model [73730](#)).

Products

1- or 2-Channel 3.6 GHz and 2- or 4-Channel 1.8 GHz, 12-bit A/D, Virtex-6 FPGA



Models 72640, 73640 and 74640 are members of the Cobalt family of high-performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71640 XMC modules mounted on a cPCI carrier board. These models include one or two 3.6 GHz, 12-bit A/D converters and four or eight banks of memory.

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The factory-installed functions of these models include one or two A/D acquisition IP

modules. In addition, IP modules for DDR3 memories, controllers for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions.

The front end accepts analog HF or IF inputs on a pair of front panel SMC connectors with transformer coupling into a Texas Instruments ADC12D1800 12-bit A/D. The converter operates in single-channel interleaved mode with a sampling rate of 3.6 GHz and an input bandwidth of 1.75 GHz; or, in dual-channel mode with a sampling rate of 1.8 GHz and input bandwidth of 2.8 GHz. The ADC12D1800 provides a programmable 15-bit gain adjustment allowing an input range of +2 to +4 dBm.

Model 72640 is a 6U cPCI board, while Model 73640 is a 3U cPCI board; Model 74640 is a dual density 6U cPCI board; also available are an XMC (Model 71640), x8 PCIe (Model 78640), 3U VPX (Models 52640 and 53640), 6U VPX (Models 57640 and 58640 dual density), and AMC (Model 56640).

Products

1- Channel 3.6 GHz or 2-Channel 1.8 GHz, 12-bit A/D, Wideband DDC, Virtex-6 FPGA

Model 56641 - AMC

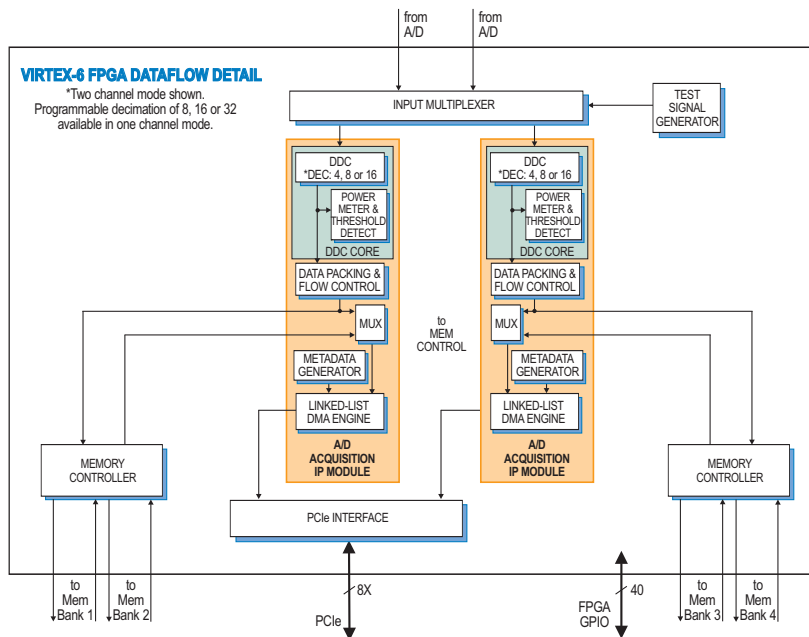


Figure 48



Model 56641
AMC



Model 56641 is a member of the Cobalt family of high-performance AMC modules based on the Xilinx Virtex-6 FPGA. A very high-speed data converter based on the Model 71640 described in the previous page, it includes additional factory-installed IP cores to enhance its performance and address the requirements of many applications.

The 56641 factory-installed functions include an A/D acquisition IP module. In addition, within the FPGA is a powerful factory-installed DDC IP core. The core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation.

In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s , where f_s is the A/D sampling frequency.

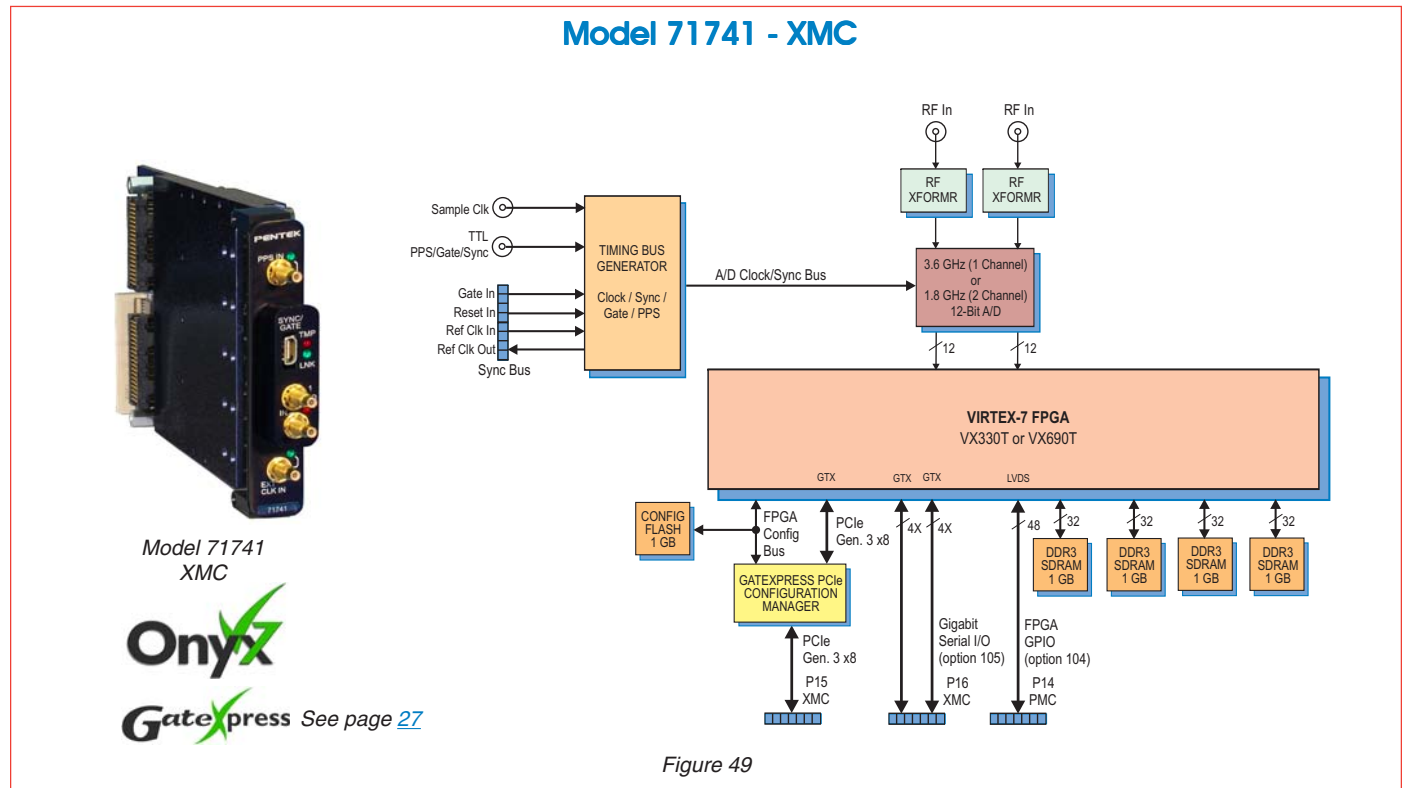
In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x.

The decimating filter for each DDC accepts a unique set of user-supplied 16-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 16-bit I + 16-bit Q samples at a rate of f_s / N .

Versions of the [56641](#) are also available as an XMC module (Model [71641](#)), x8 PCIe board (Model [78641](#)), 3U VPX (Models [52641](#) and [53641](#)), 6U VPX (Models [57641](#) and [58641](#) dual density), 6U cPCI (Models [72641](#) and [74641](#) dual density), and 3U cPCI (Model [73641](#)).

Products

1-Channel 3.6 GHz or 2-Channel 1.8 GHz, 12-bit A/D, Wideband DDC, Virtex-7 FPGA



Model 71741 is a member of the Onyx family of high-performance XMC modules based on the Xilinx Virtex-7 FPGA. A high-speed data converter with a programmable digital downconverter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution. It includes a 3.6 GHz, 12-bit A/D converter and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, Model 71741 includes an optional connection to the Virtex-7 FPGA for custom I/O.

The Pentek Onyx architecture features a Virtex-7 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

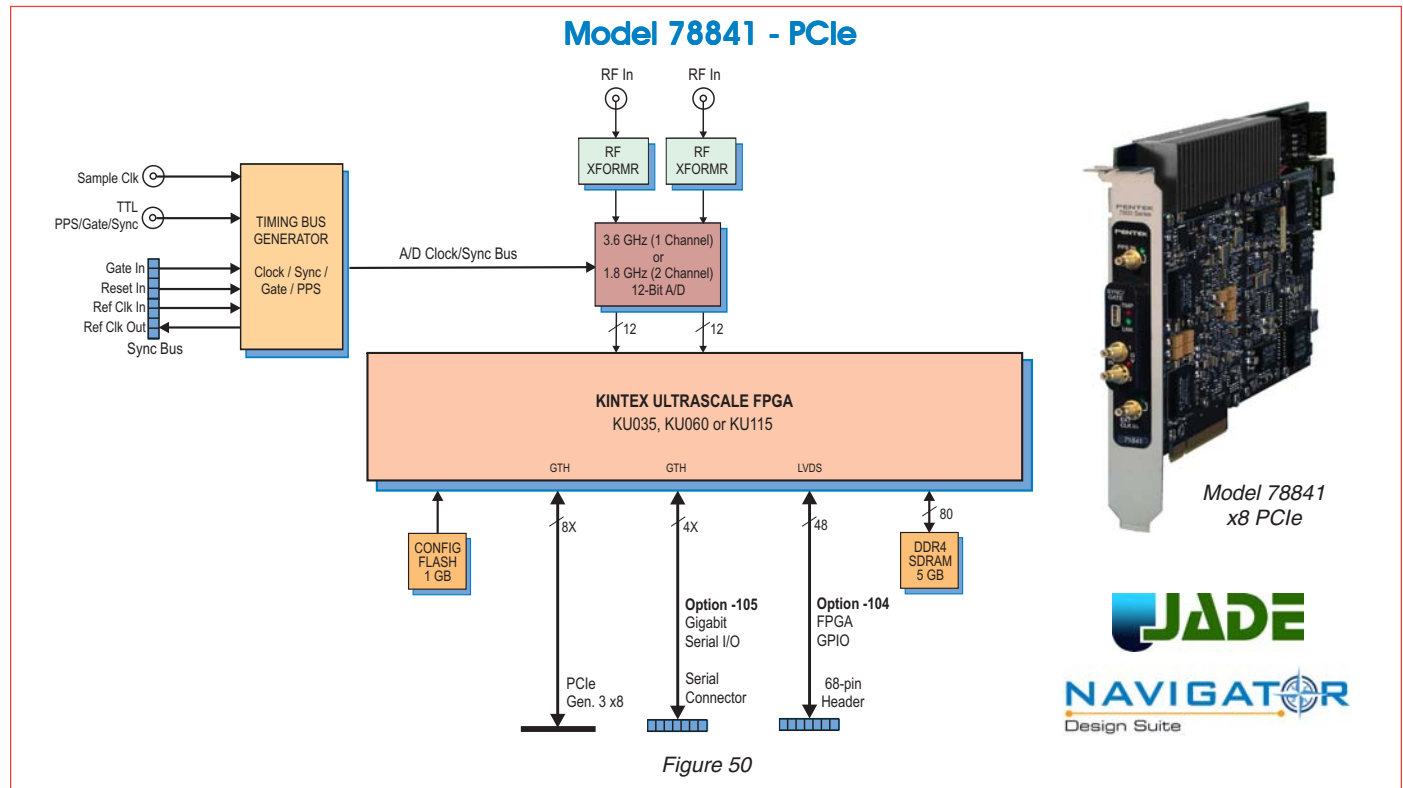
The 71741 factory-installed functions include an A/D acquisition IP module and a programmable digital downconverter.

The DDC core supports a single-channel mode, accepting data samples from the A/D at the full 3.6 GHz rate. Additionally, a dual-channel mode supports the A/D's 1.8 GHz two-channel operation. In dual-channel mode, each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s . In single-channel mode, decimation can be programmed to 8x, 16x or 32x. In dual-channel mode, both channels share the same decimation rate, programmable to 4x, 8x or 16x. See the dataflow diagram of the 71641 on the previous page for more detail.

Versions of the [71741](#) are also available as an x8 PCIe half-length board (Model [78741](#)), 3U VPX (Models [52741](#) and [53741](#)), 6U VPX (Models [57741](#) and [58741](#) (dual density), AMC (Model [56741](#)), 6U cPCI (Models [72741](#) and [74721](#) with dual density), and 3U cPCI (Model [73741](#)).

Products

1-Channel 3.6 GHz or 2-Channel 1.8 GHz, 12-bit A/D, Wideband DDC, Kintex UltraScale FPGA



Model 78841 is a member of the Jade™ family of high-performance PCIe boards. The Jade architecture embodies a new stream-lined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 78841 is a high-speed data converter with programmable DDCs). It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes a 3.6 GHz, 12-bit A/D converter and a large DDR4 memory. In addition to supporting PCI Express

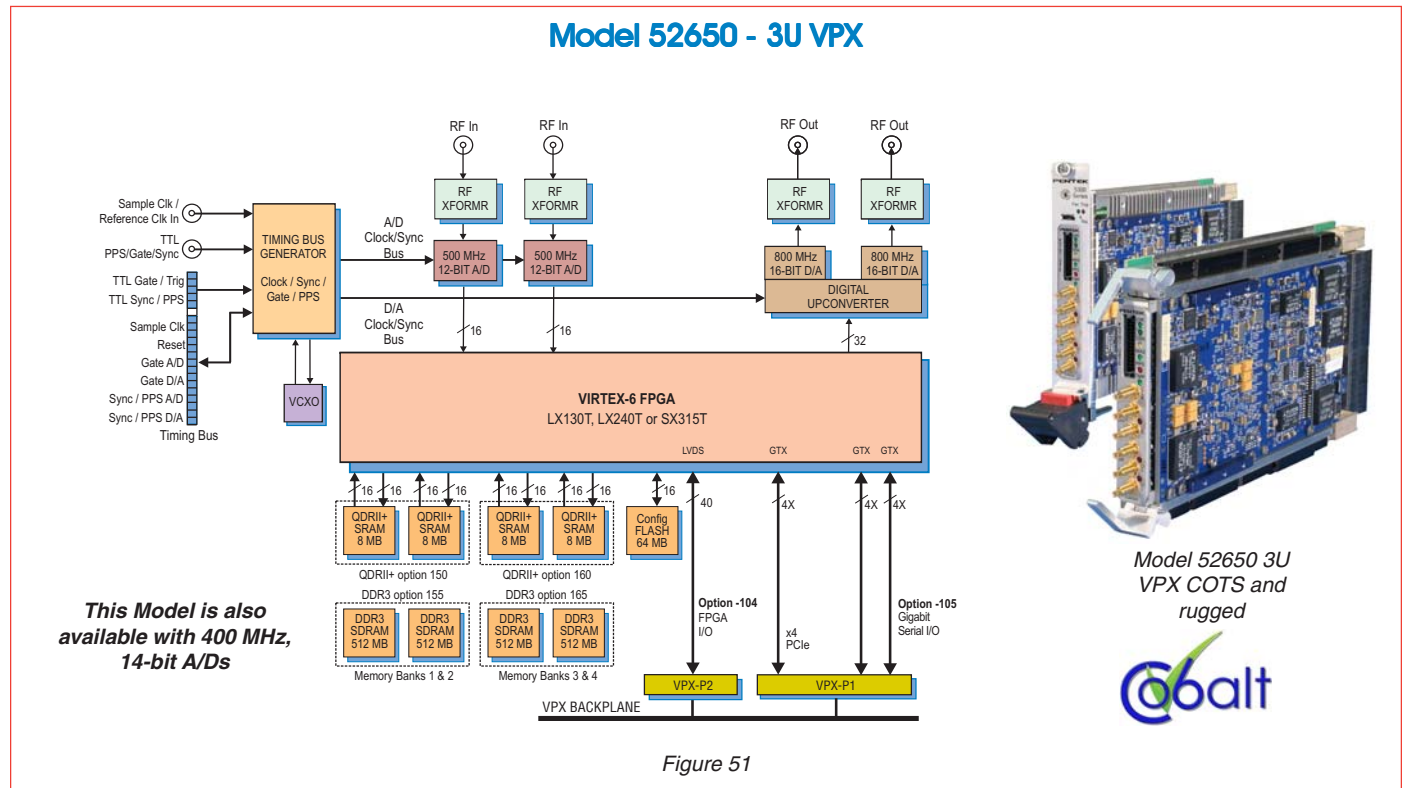
Gen. 3 as a native interface, Model 78841 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 78841 factory-installed functions include an A/D acquisition IP module and a programmable digital downconverter. In addition, IP modules for DDR4 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable the 78841 to operate as a complete turnkey solution, without the need to develop any FPGA IP.

Versions of the [78841](#) are also available as an XMC module (Model [71841](#)), 3U VPX (Models [52841](#) and [53841](#)), 6U VPX (Models [57841](#) and [58841](#) with dual density), AMC (Model [56841](#)), 6U cPCI (Models [72841](#) and [74841](#) with dual density), and 3U cPCI (Model [73841](#)).

Products

2-Channel 500 MHz A/D, DUC, 2-Channel 800 MHz D/A, Virtex-6 FPGA



Model 52650 is a member of the Cobalt family of high-performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A two-channel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. The 52650 includes two 500 MHz 12-bit A/Ds, one DUC, two 800 MHz 16-bit D/As and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

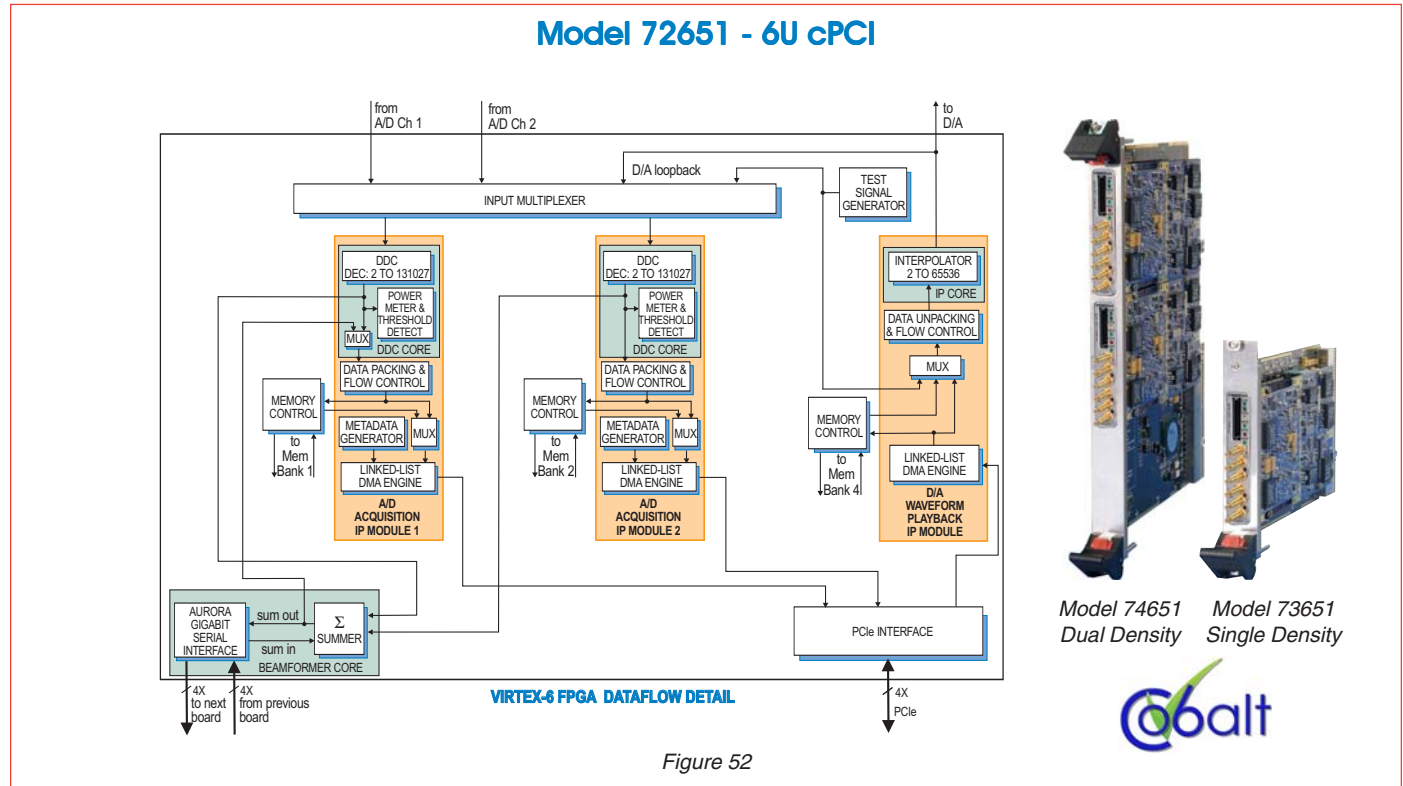
Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 52650 factory-installed functions include an A/D acquisition and a D/A waveform playback IP module. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions.

Multiple 52650's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards. The architecture supports up to four memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combinations.

Versions of the [52650](#) are also available as a 3U VPX (Model [53650](#)), 6U VPX (Models [57650](#) and [58650](#) dual density), XMC module (Model [71650](#)), an x8 PCIe board (Model [78650](#)), AMC (Model [56650](#)), 6U cPCI (Models [72650](#) and [74650](#) dual density), and 3U cPCI (Model [73650](#)).

Products

2- or 4-Channel 500 MHz A/D, with DDCs, DUCs, 2- or 4-Channel 800 MHz D/A, Virtex-6 FPGA



Models 72651, 73651 and 74651 are members of the Cobalt family of high-performance CompactPCI boards based on the Xilinx Virtex-6 FPGA. They consist of one or two Model 71651 XMC modules mounted on a cPCI carrier board. These models include two or four A/Ds, two or four multiband DDCs, one or two DUCs, two or four D/As and three or six banks of memory.

These models feature two or four A/D Acquisition IP modules for easily capturing and moving data. Each module can receive data from either of the two A/Ds, a test signal generator or from the D/A Waveform Playback IP module in loopback mode.

Within each A/D Acquisition IP Module is a powerful DDC IP core. Because of the flexible input routing of the A/D Acquisition IP Modules, many different configurations can be achieved including one A/D driving both DDCs or each of the two A/Ds driving its own DDC.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s , where f_s is

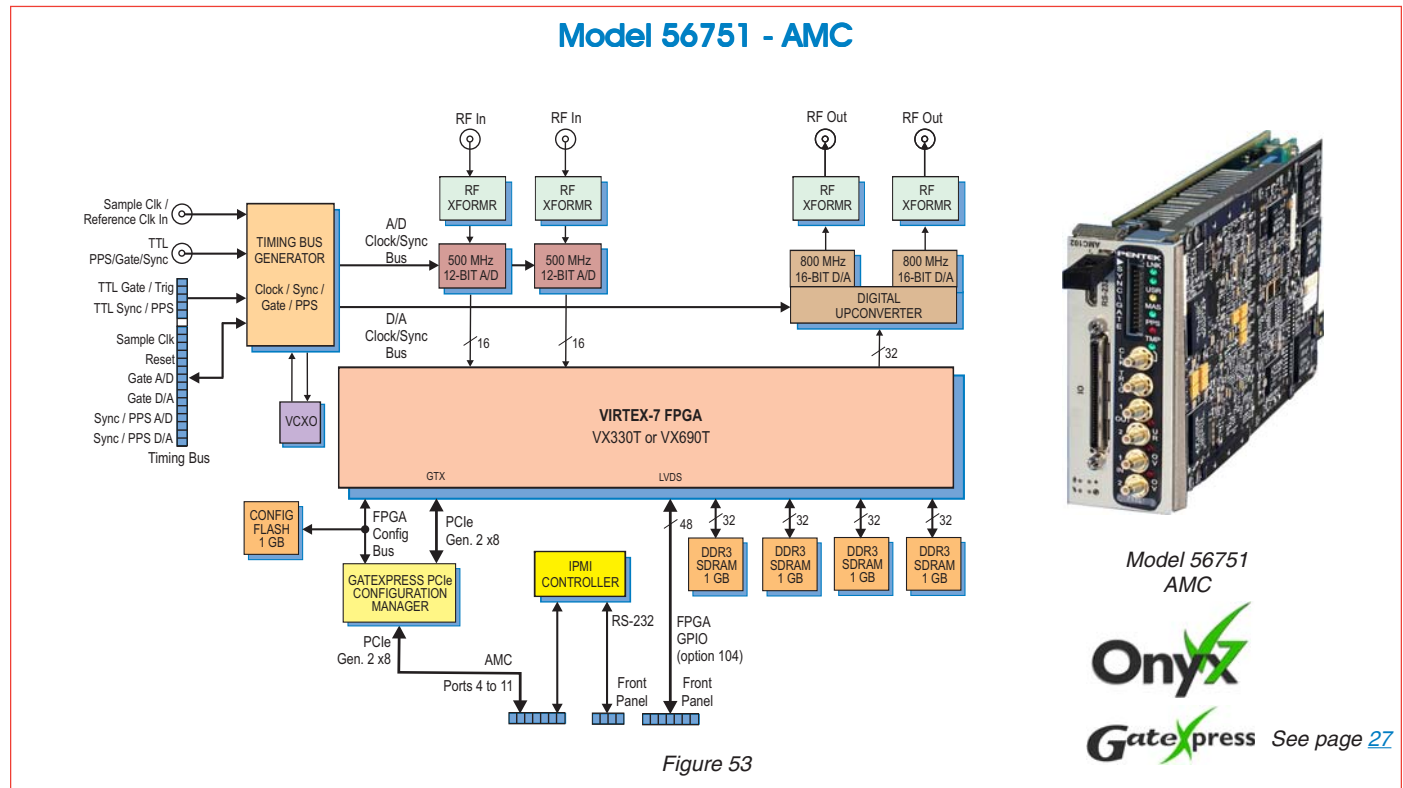
the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as two or four different output bandwidths for the board. Decimations can be programmed from 2 to 131,072 providing a wide range to satisfy most applications.

In addition to the DDCs, these models feature one or two complete beamforming subsystems. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The time constant of the averaging interval for each meter is programmable up to 8K samples. The power meters present average power measurements for each DDC core output.

Model [72651](#) is a 6U cPCI board, while Model [73651](#) is a 3U cPCI board; Model [74651](#) a dual density 6U cPCI board; also available are an XMC (Model [71651](#)), an x8 PCIe (Model [78651](#)), 3U VPX (Models [52651](#) and [53651](#)), 6U VPX (Models [57651](#) and [58651](#) dual density), and AMC (Model [56651](#)).

Products

2-Channel 500 MHz A/D, with DDCs, DUCs, 2-Channel 800 MHz D/A, Virtex-7 FPGA



Model 56751 is a member of the Onyx family of high-performance AMC modules based on the Xilinx Virtex-7 FPGA. A multichannel, high-speed data converter with a programmable DDC, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. It includes two A/Ds, two D/As and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 56751 includes a general-purpose front-panel connector for application-specific I/O.

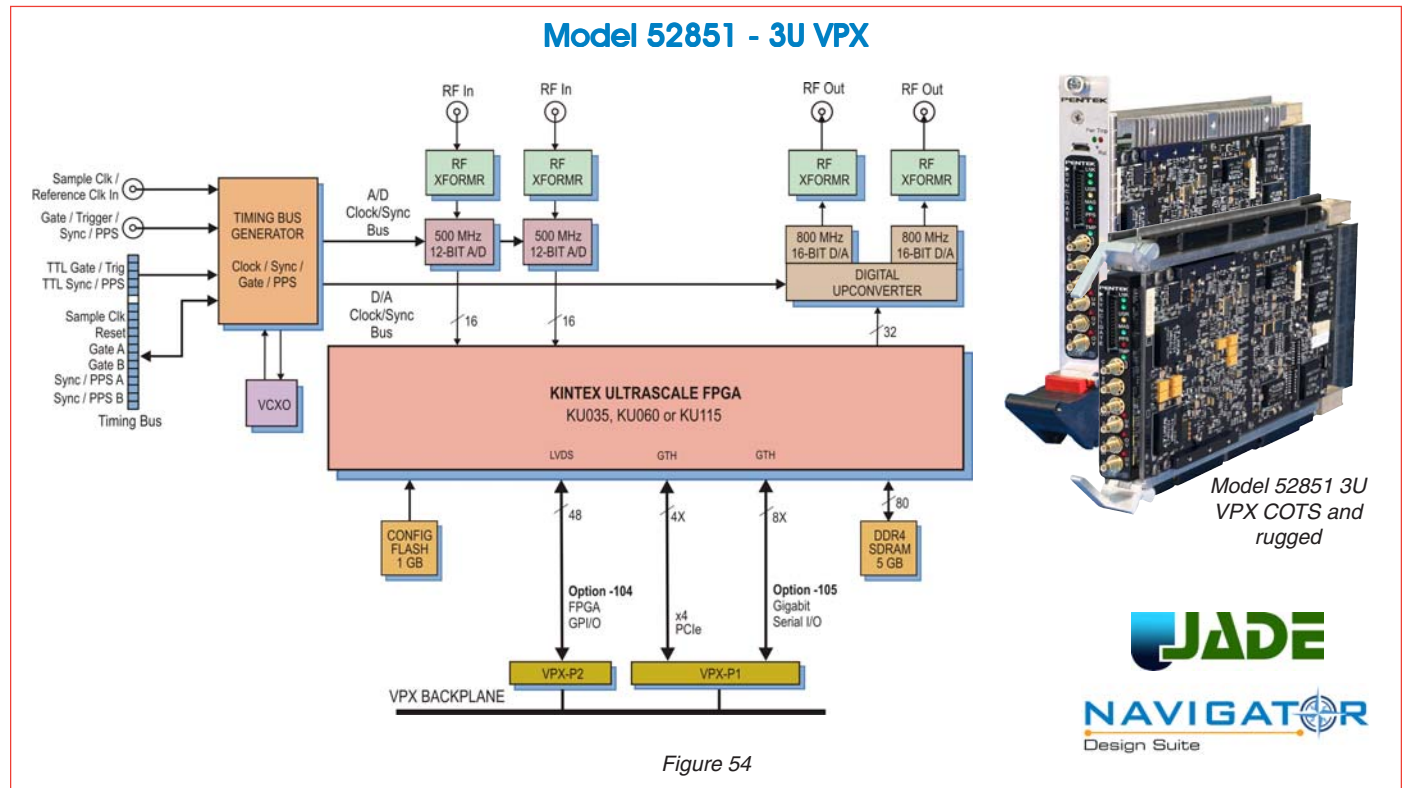
The Pentek Onyx architecture features a Virtex-7 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 56751 factory-installed functions include two A/D acquisition and a D/A waveform playback IP modules. Each of the two acquisition IP modules contains a powerful, programmable DDC IP core. The waveform playback IP module contains an interpolation IP core, ideal for matching playback rates to the data and decimation rates of the acquisition modules. IP modules for DDR3 memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 56751 to operate as a turnkey solution. See the block diagram on the previous page for more detail.

Versions of the [56751](#) are also available as an XMC module (Model [71751](#)), x8 PCIe board (Model [78751](#)), 3U VPX (Models [52751](#) and [53751](#)), 6U VPX (Models [57751](#) and [58751](#) dual density), 6U cPCI (Models [72751](#) and [74751](#) dual density), and 3U cPCI (Model [73751](#)).

Products

2-Channel 500 MHz A/D, with DDCs, DUCs, 2-Channel 800 MHz D/A, Kintex UltraScale FPGA



Model 52851 is a member of the Jade™ family of high-performance 3U VPX boards. The Jade architecture embodies a new stream-lined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 52851 is a 2-channel, high-speed data converter with programmable DDCs. It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes two A/Ds, a complete multiboard clock and sync section, a large DDR4 memory, two DDCs, one DUC and two D/As. In addition to supporting PCI Express

Gen. 3 as a native interface, the Model 52851 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

The 52851 factory-installed functions include two A/D acquisition and a waveform playback IP module for simplifying data capture and playback, and data transfer between the board and a host computer.

Additional IP includes: a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; two test signal generators; a programmable interpolator, and a PCIe interface. These complete the factory-installed functions and enable the 52851 to operate as a complete turnkey solution for many applications.

Versions of the [52851](#) are also available as a 3U VPX (Model [53851](#)), 6U VPX (Models [57851](#) and [58851](#) dual density), XMC module (Model [71851](#)), a PCIe board (Model [78851](#)), AMC (Model [56851](#)), 6U cPCI (Models [72851](#) and [74851](#) dual density), and 3U cPCI (Model [73851](#)).

Products

4-Channel 200 MHz 16-bit A/D with Virtex-6 FPGA

Model 71660 - XMC

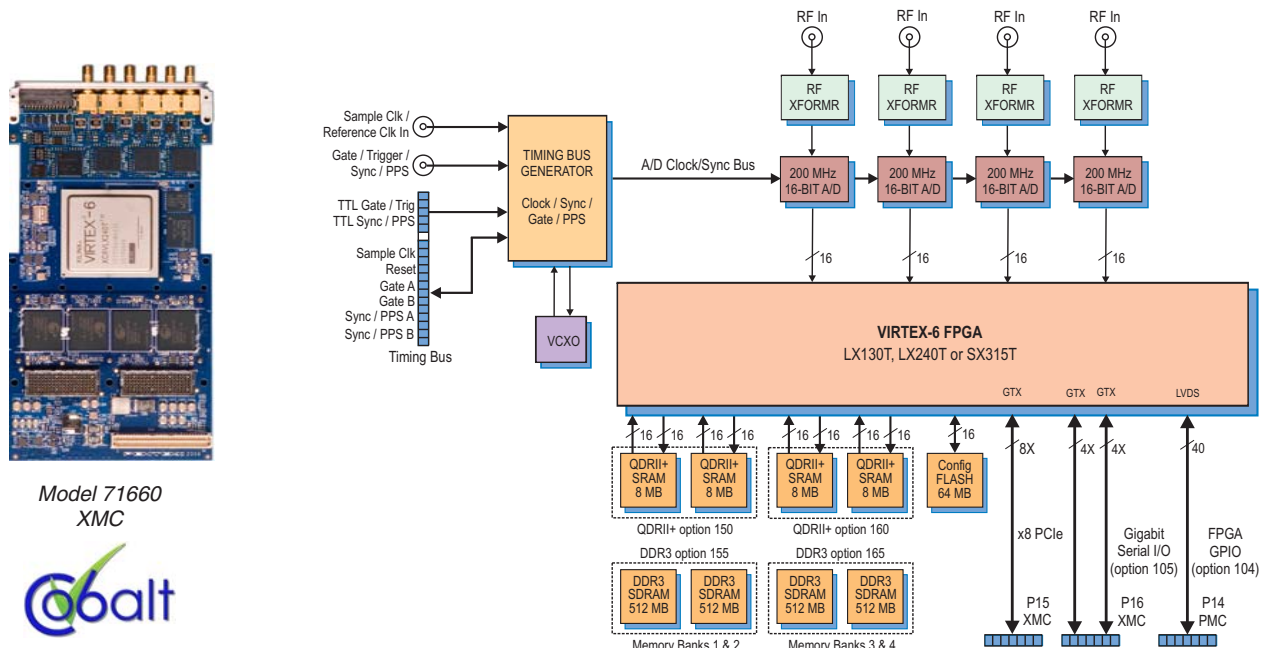


Figure 55

Model 71660 is a member of the Cobalt family of high-performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. It includes four 200 MHz, 16-bit A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 71660 includes general purpose and gigabit serial connectors for application-specific I/O.

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

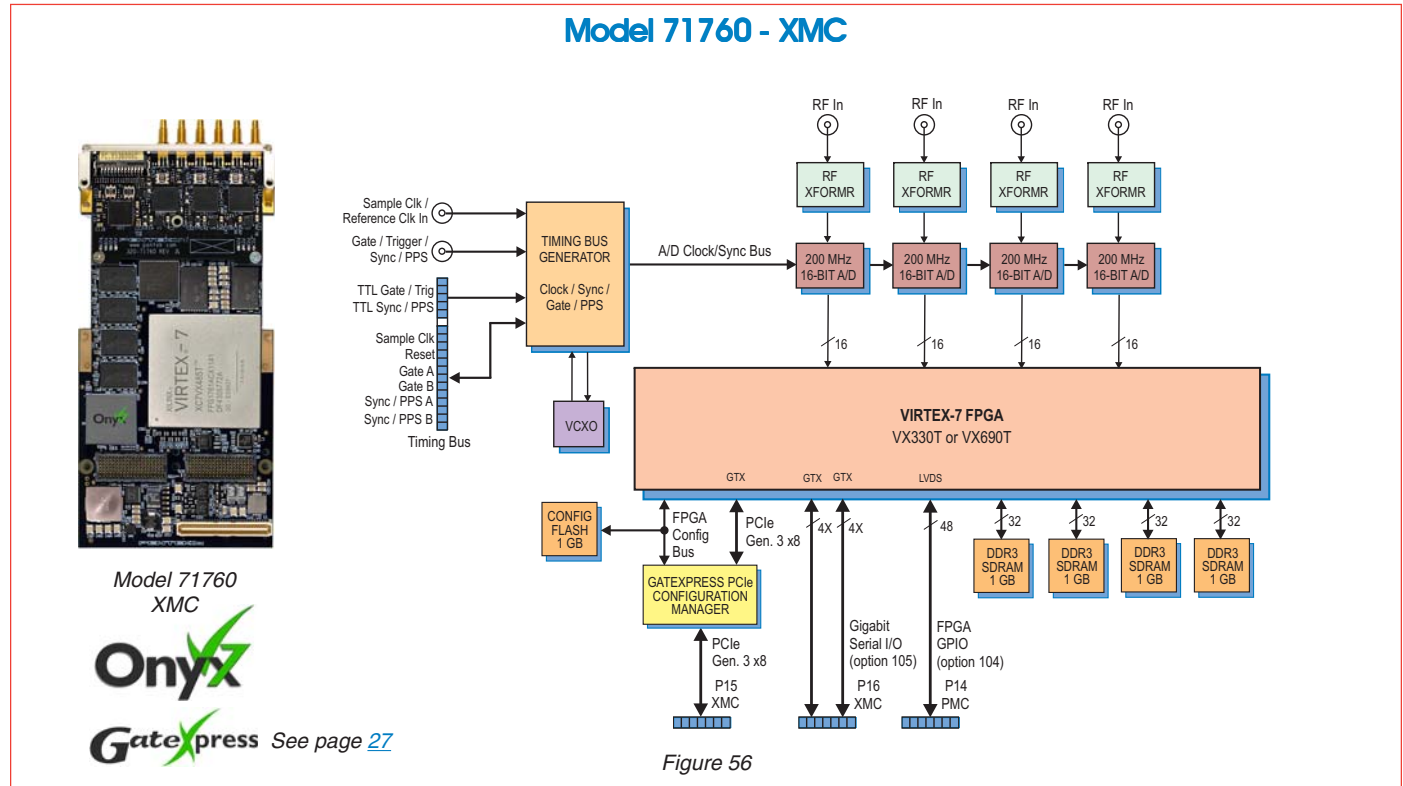
Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71660 factory-installed functions include four A/D acquisition IP modules. In addition, IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions.

Multiple 71660's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected modules. The architecture supports up to four memory banks which can be configured with all QDRII+ SRAM, DDR3 SDRAM, or as combination of two banks of each type of memory.

Versions of the [71660](#) are also available as an x8 PCIe half-length board (Model [78660](#)), 3U VPX (Models [52660](#) and [53660](#)), 6U VPX (Models [57660](#) and [58660](#) dual density), AMC (Model [56660](#)), 6U cPCI (Models [72660](#) and [74660](#) with dual density), and 3U cPCI (Model [73660](#)).

Products

4-Channel 200 MHz, 16-bit A/D with Virtex-7 FPGA



Model 71760 is a member of the Onyx family of high-performance XMC modules based on the Xilinx Virtex-7 FPGA. A multichannel, high-speed data converter, it is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP. It includes four A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71760 includes general purpose and gigabit serial connectors for application-specific I/O.

Based on the proven design of the Pentek Cobalt family, Onyx raises the processing performance with the new flagship family of Virtex-7 FPGAs from Xilinx. As the central feature of the board architecture, the FPGA has access to all data and control paths, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

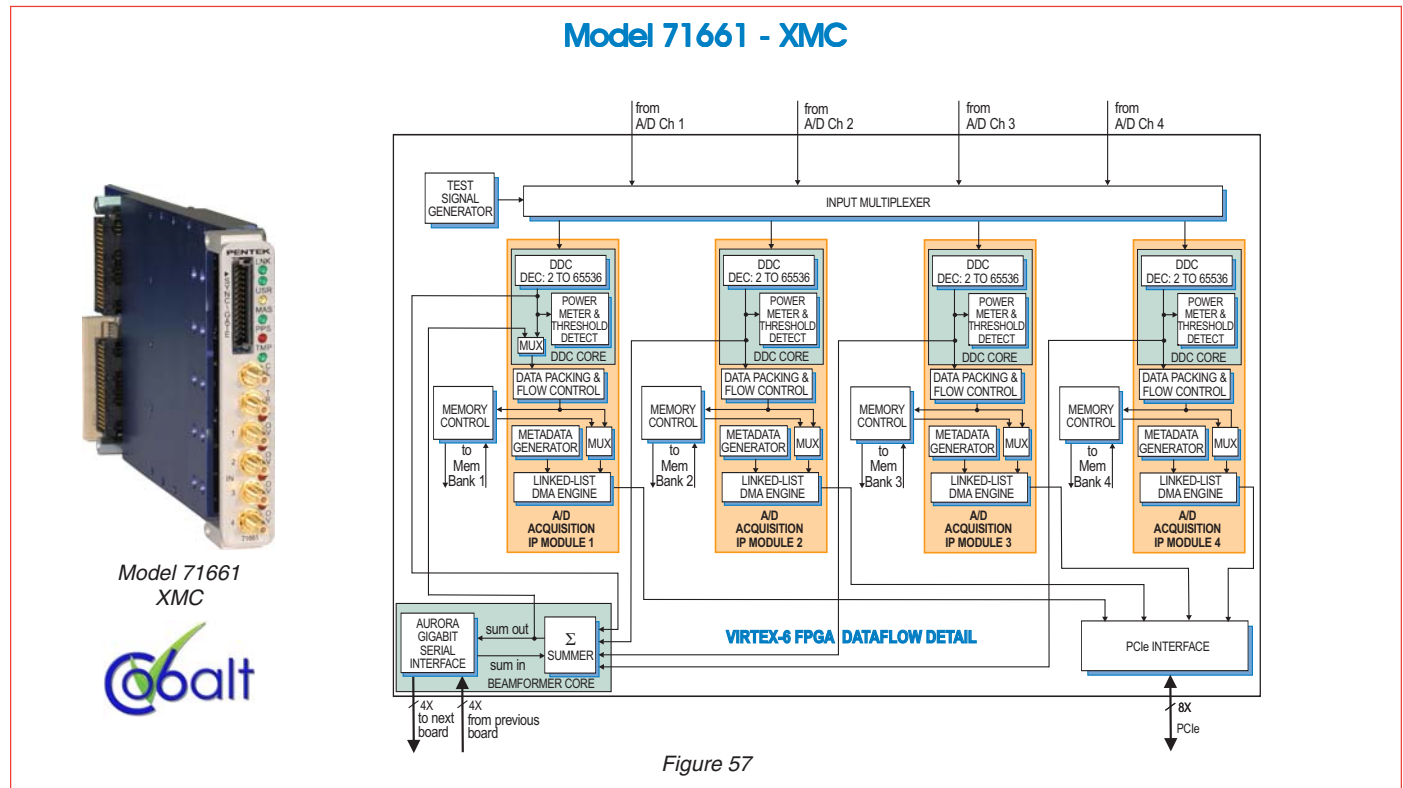
Each member of the Onyx family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71760 factory-installed functions include four A/D acquisition IP modules for simplifying data capture and data transfer. IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions.

The 71760 architecture supports four independent DDR3 SDRAM memory banks. Each bank is 1 GB deep and is an integral part of the module's DMA capabilities, providing FIFO memory space for creating DMA packets. Built-in memory functions include multichannel A/D data capture, tagging and streaming.

Versions of the [71760](#) are also available as an x8 PCIe half-length board (Model [78760](#)), 3U VPX (Models [52760](#) and [53760](#)), 6U VPX (Models [57760](#) and [58760](#) (dual density), AMC (Model [56760](#)), 6U cPCI (Models [72760](#) and [74760](#) dual density), and 3U cPCI (Model [73760](#)).

Products

4-Channel 200 MHz 16-bit A/D with Installed IP Cores, Virtex-6 FPGA



Model 71661 is a member of the Cobalt family of high-performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter based on the Model 71660 described in the previous page, it includes factory-installed IP cores to enhance the performance of the 71620 and address the requirements of many applications.

The 71661 factory-installed functions include four A/D acquisition IP modules. Each of the four acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s , where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as four different output bandwidths for the board. Decimations

can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The 71661 also features a complete beamforming subsystem. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The power meters present average power measurements for each DDC core output in easy-to-read registers. A threshold detector automatically sends an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

For larger systems, multiple 71661's can be chained together via the built-in Xilinx Aurora gigabit serial interface through the P16 XMC connector.

Versions of the [71661](#) are also available as an x8 PCIe half-length board (Model [78661](#)), 3U VPX (Models [52661](#) and [53661](#)), 6U VPX (Models [57661](#) and [58661](#) dual density), AMC (Model [56661](#)), 6U cPCI (Models [72661](#) and [74661](#) with dual density), and 3U cPCI (Model [73661](#)).

Products

4-Channel 200 MHz 16-bit A/D with Installed IP Cores, Virtex-7 FPGA

Model 58761 - 6U VPX, Dual Density

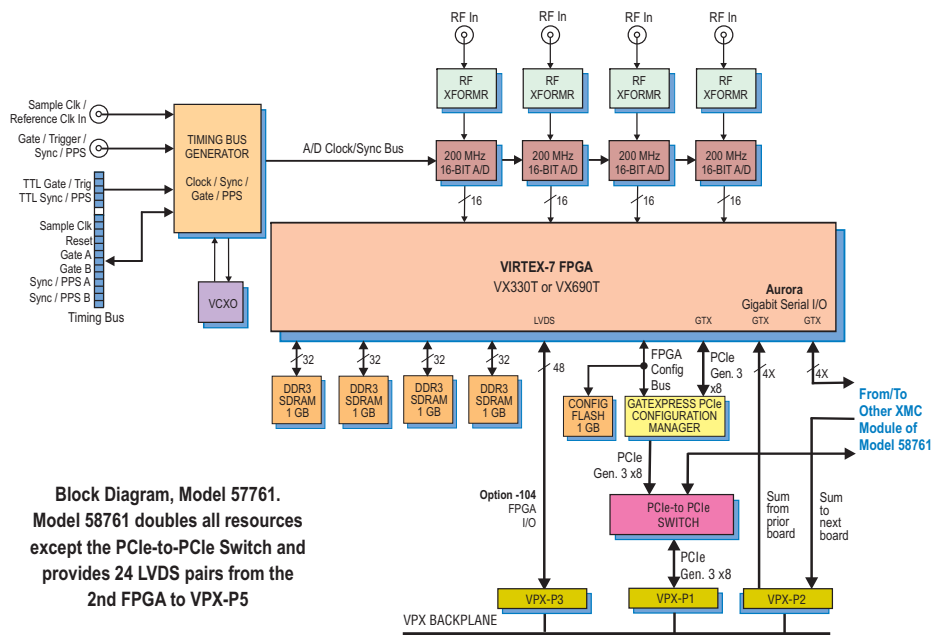


Figure 58


 Model 58761
 6U VPX
 dual density


See page 27

Model 58761 is a member of the Onyx family of high-performance VPX boards based on the Xilinx Virtex-7 FPGA. A multichannel, high-speed data converter based on the Model 71760 described previously, it includes factory-installed IP cores to enhance the performance of the 71760 and address the requirements of many applications.

The 58761 factory-installed functions include eight A/D acquisition IP modules. Each of the acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for DDR3 memories, controllers for all data clocking and synchronization functions, test signal generators, Aurora gigabit serial interfaces, and a PCIe interface complete the factory-installed functions.

Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s , where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as eight different output bandwidths for the board. Decima-

tions can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

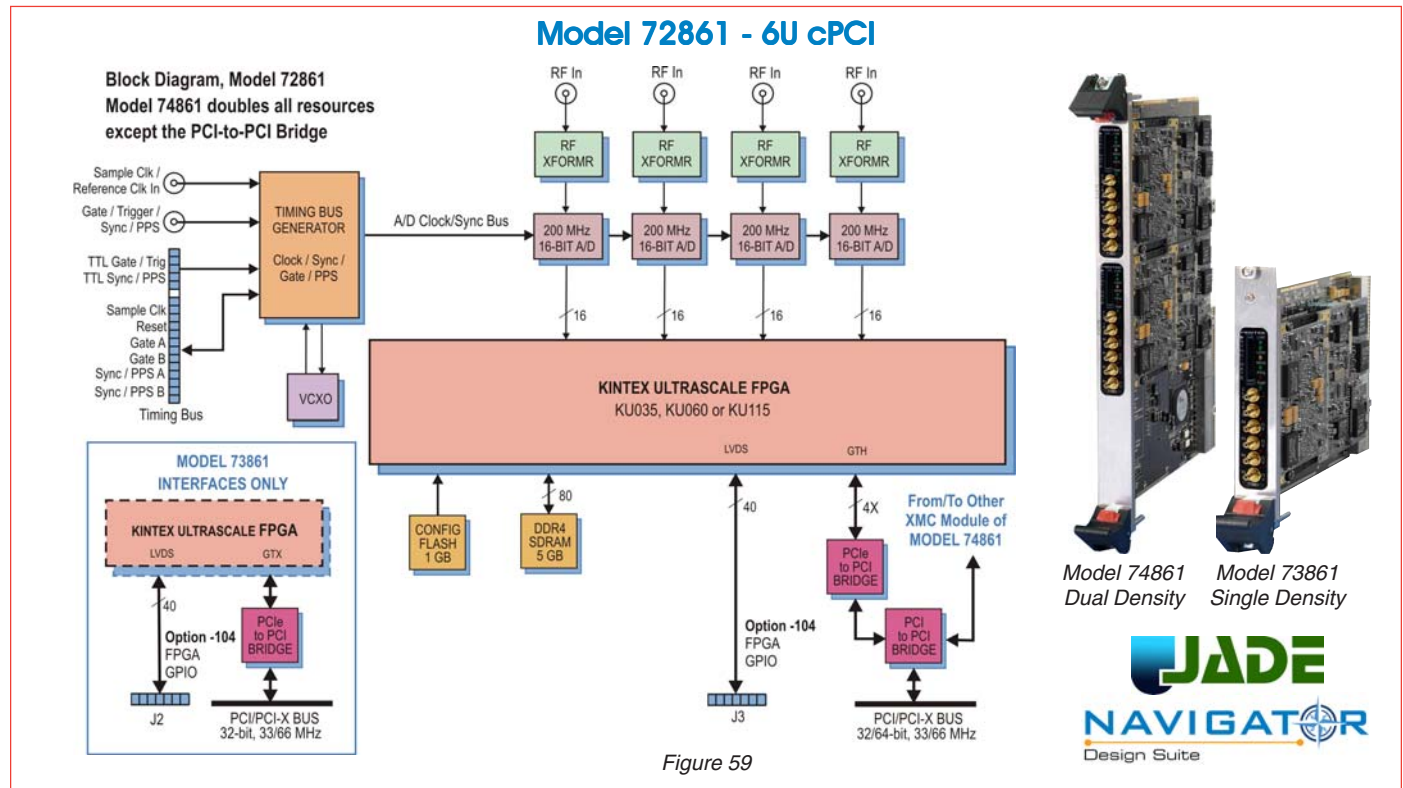
The 58761 also features two complete beamforming subsystems. Each DDC core contains programmable I & Q phase and gain adjustments followed by a power meter that continuously measures the individual average power output. The power meters present average power measurements for each DDC core output in easy-to-read registers. A threshold detector automatically sends an interrupt to the processor if the average power level of any DDC core falls below or exceeds a programmable threshold.

For larger systems, multiple 58761's can be chained together via the built-in Xilinx Aurora gigabit serial interfaces.

Versions of the [58761](#) are also available as XMC (Model [71761](#)), x8 PCIe half-length board (Model [78761](#)), 3U VPX (Models [52761](#) and [53761](#)), 6U VPX (Model [57761](#) single density), AMC (Model [56761](#)), 6U cPCI (Models [72761](#) and [74761](#) dual density), and 3U cPCI (Model [73761](#)).

Products

4-Channel 200 MHz 16-bit A/D with Installed IP Cores, Kintex Ultrascale FPGA



Models 72861, 73861 and 74861 are members of the Jade™ family of high-performance CompactPCI (cPCI) boards. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

These models consist of one or two Model 71861 XMC modules mounted on a cPCI carrier board. Model 72861 is a 6U board while Model 73861 is a 3U board; both have one Model 71861 module. Model 74861 is equipped with two XMC modules rather than one.

The cPCI models include four or eight A/Ds, complete multiboard clock and sync sections, and large DDR4 memories. Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces.

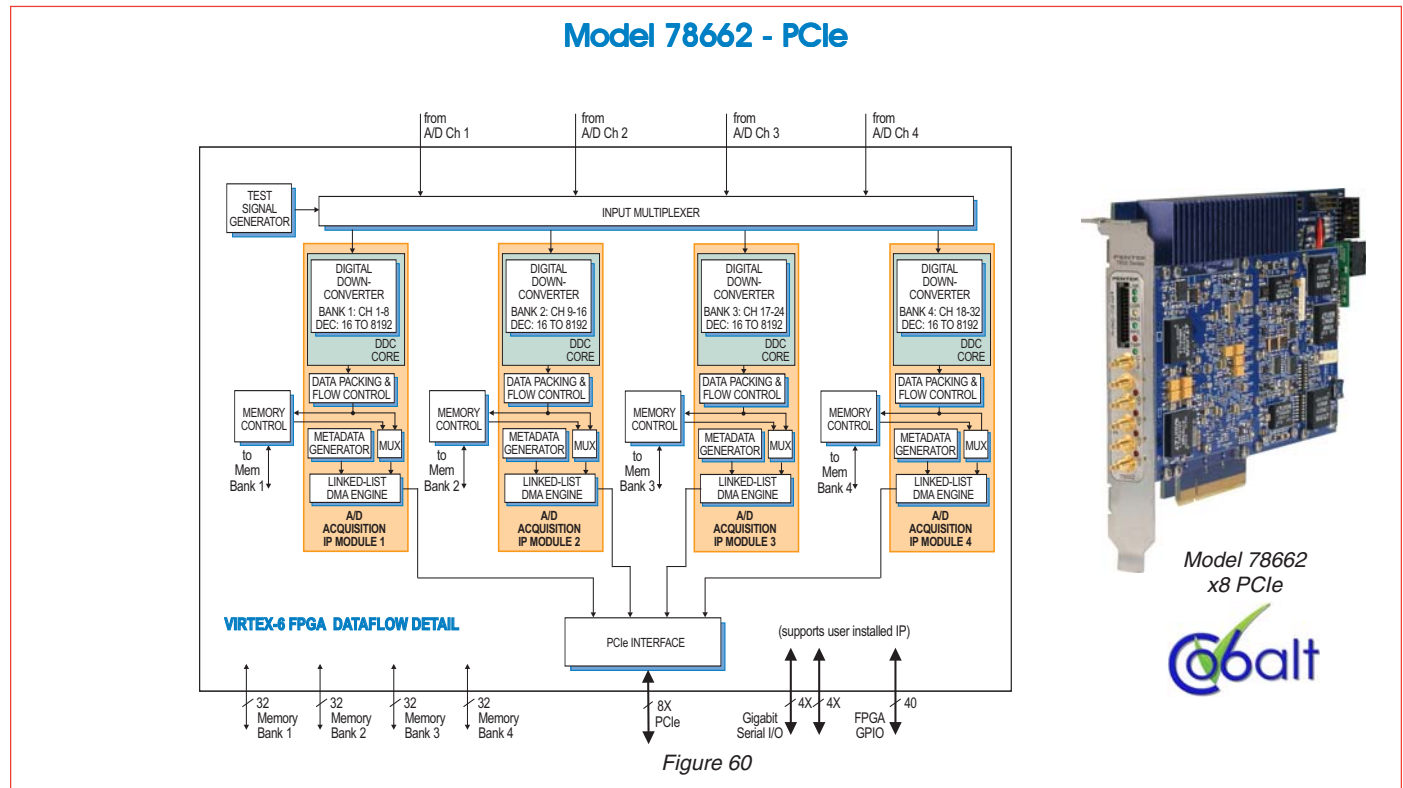
The factory-installed functions include four or eight A/D acquisition IP modules for simplifying data capture and transfer.

Each of the acquisition IP modules contains a powerful, programmable DDC IP core; IP modules for DDR4 SDRAM memory; controllers for all data clocking and synchronization functions; test signal generators; and a PCIe interface. These complete the factory-installed functions and enable these models to operate as complete turnkey solutions for many applications. The architecture supports 5 or 10 GB banks of DDR4 SDRAM memory. User-installed IP along with the Pentek-supplied DDR4 controller core within the FPGA can take advantage of the memory for custom applications.

Model [72861](#) is a 6U cPCI board, while Model [73861](#) is a 3U cPCI board; Model [74861](#) is a dual density 6U cPCI board; also available are an XMC (Model [71861](#)), x8 PCIe (Model [78861](#)), 3U VPX (Models [52861](#) and [53861](#)), 6U VPX (Models [57861](#) and [58861](#) dual density), and AMC (Model [56861](#)).

Products

4-Channel 200 MHz 16-bit A/D with Installed IP Cores, Virtex-6 FPGA



Model 78662 is a member of the Cobalt family of high-performance PCIe boards based on the Xilinx Virtex-6 FPGA. Based on the Model 71660 presented previously, this four-channel, high-speed data converter with programmable DDCs is suitable for connection to HF or IF ports of a communications or radar system.

The 78662 factory-installed functions include four A/D acquisition IP modules. Each of the four acquisition IP modules contains a powerful, programmable 8-channel DDC IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, voltage and temperature monitoring, and a PCIe interface complete the factory-installed functions.

Each of the 32 DDC channels has an independent 32-bit tuning frequency setting that ranges from DC to f_s , where f_s is the A/D sampling frequency. All of the 8 channels within a bank share a common decimation setting ranging from 16 to 8192. Each 8-channel bank

can have its own unique decimation setting supporting a different bandwidth associated with each of the four acquisition modules.

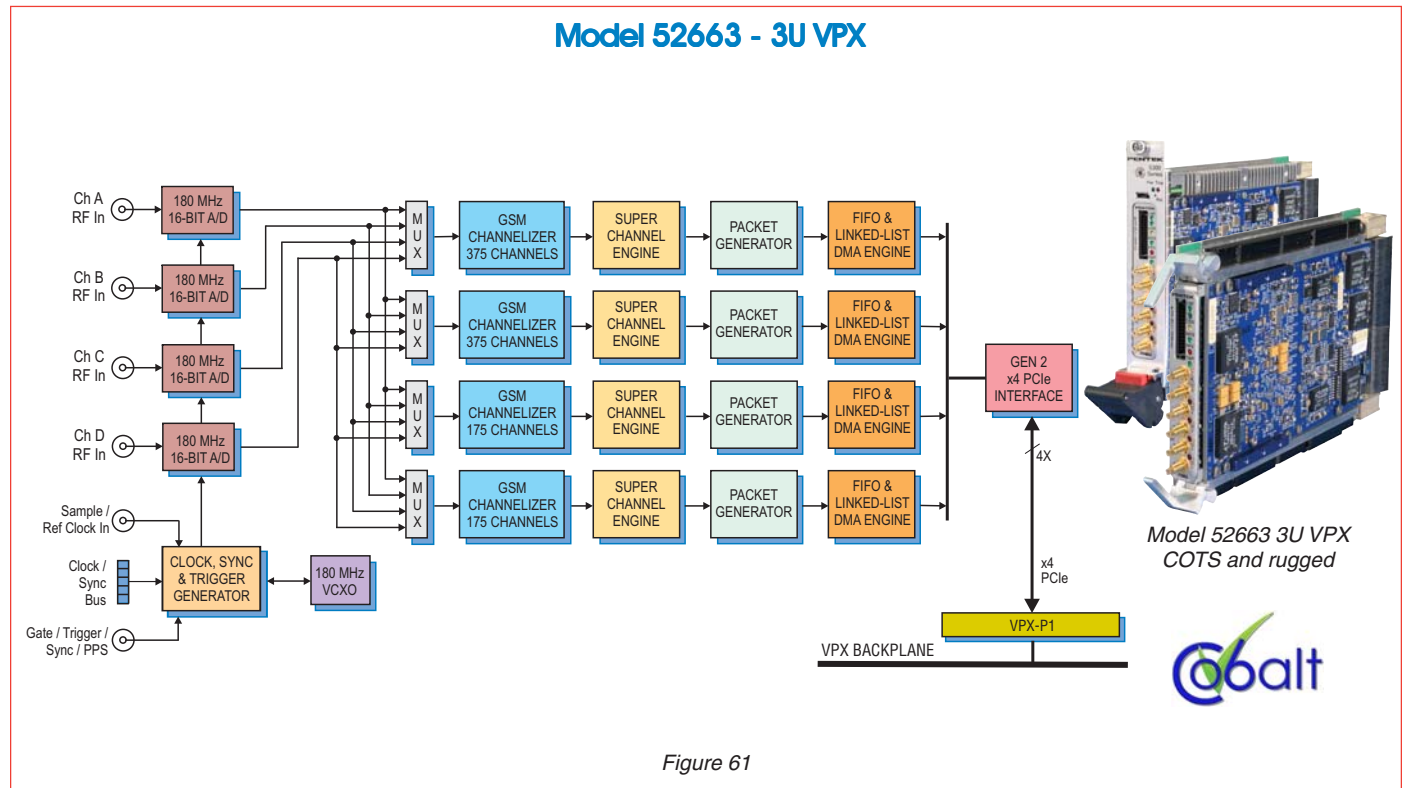
The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s / N . Any number of channels can be enabled within each bank, selectable from 0 to 8. Multiple 78662's can be driven from the LVPECL bus master, supporting synchronous sampling and sync functions across all connected boards.

Versions of the [78662](#) are also available as an XMC module (Model [71662](#)), 3U VPX (Models [52662](#) and [53662](#)), 6U VPX (Models [57662](#) and [58662](#) with dual density), AMC (Model [56662](#)), 6U cPCI (Models [72662](#) and [74662](#) with dual density), and 3U cPCI (Model [73662](#)).

Products

1100-Channel GSM Channelizer with Quad A/D, Virtex-6 FPGA



The Model 52663 accepts four analog inputs from an external analog RF tuner, such as the Pentek Model 8111, where the GSM RF bands are downconverted to an IF frequency. These IF signals are then digitized by four A/D converters and routed to four channelizer banks, which perform digital downconversion of all GSM channels to baseband. Two of the banks handle 175 channels for the lower GSM transmit/receive bands and two more banks handle 375 channels for the upper bands. The DDC channels within each bank are equally spaced at 200 kHz.

Each DDC output is resampled to a 4x symbol rate of 1.08333 MHz to simplify symbol recovery. Every four DDC outputs are combined into a frequency-division “super-channel” that allows transmission of all 1100 channels across the PCIe Gen. 2 x4 interface. The GSM channelizer IP core is supported with factory-installed FPGA functions including packet formation, time stamping, four DMA controllers, gating and triggering.

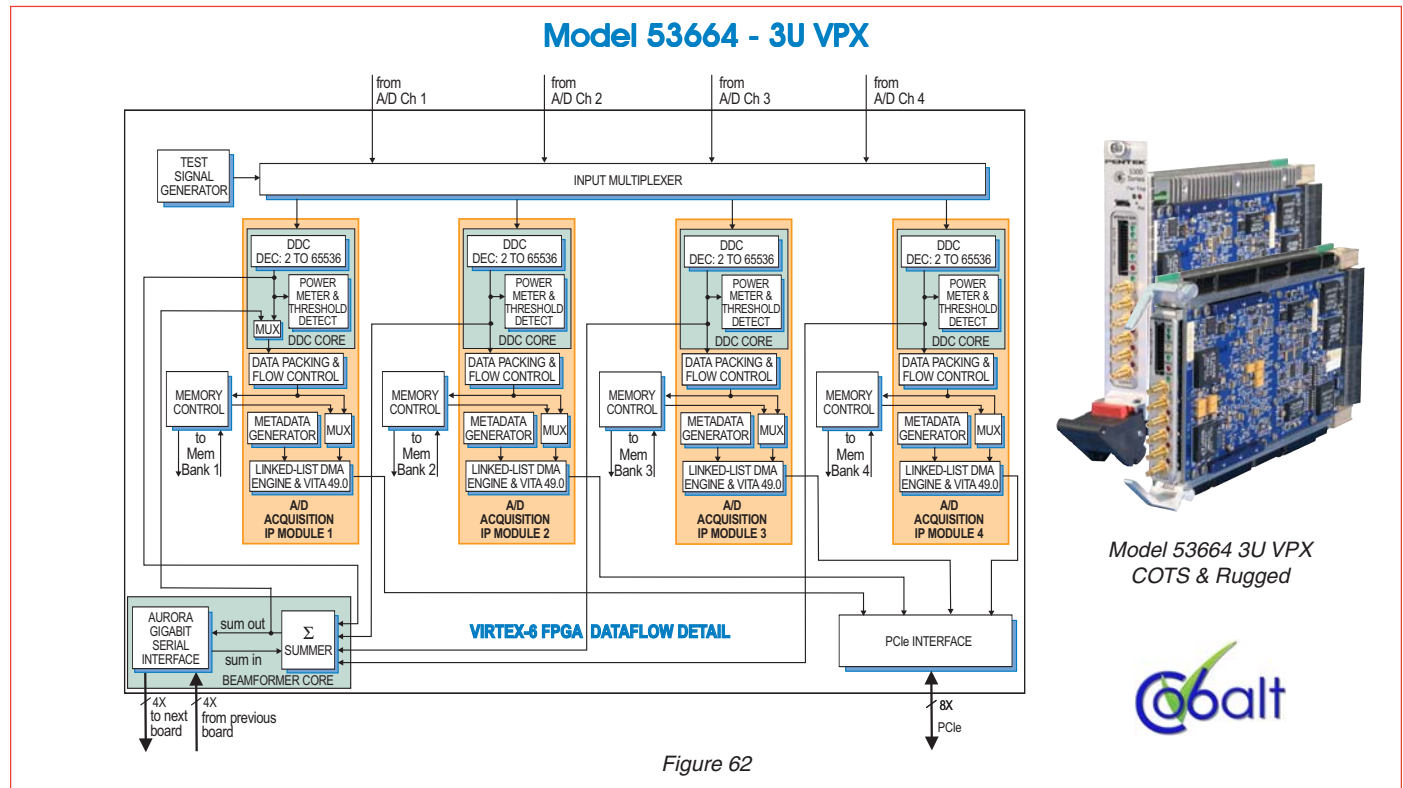
Super-channel packets are formed by appending enabled super-channel samples sequentially from each bank. Once complete, a unique super-channel packet header is inserted at the beginning of each packet for identification. The header contains a time stamp, a sequential packet count, the number of enabled super-channels, the DMA channel identifier, and other information.

The 52663 is ideal for mobile monitoring systems that must capture some or all of the 1100 uplink and downlink signals in both upper and lower GSM bands. This full-global system for mobile communications spectrum monitoring targets homeland security, government and military applications.

Versions of the [52633](#) are also available as an XMC module (Model [71663](#)), an x8 PCIe half-length board (Model [78663](#)), 3U VPX (Model [53663](#)), 6U VPX (Models [57663](#) and [58663](#) with dual density), AMC (Model [56663](#)), 6U cPCI (Models [72663](#) and [74663](#) with dual density), and 3U cPCI (Model [73663](#)).

Products

4-Channel 200 MHz 16-bit A/D with Installed DDC and VITA 49.0 IP Cores, Virtex-6 FPGA



Model 53664 is a member of the Cobalt family of high-performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter based on the Model 71660 described previously, it includes a programmable DDC and is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution. The 53664 PCIe output supports fully the VITA 49.0 VITA Radio Transport (VRT) Standard described on page 20.

The 53664 factory-installed functions include four A/D acquisition IP modules. Each of the four acquisition IP modules contains a powerful, programmable DDC IP core. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, an Aurora gigabit serial interface, and a PCIe interface complete the factory-installed functions.

The VITA 49.0 specification addresses the problem of interoperability between different elements of Software

Defined Radio (SDR) systems. Specifically, each SDR receiver manufacturer typically develops custom and proprietary digitized data and metadata formats, making interoperability of data from different receivers impossible.

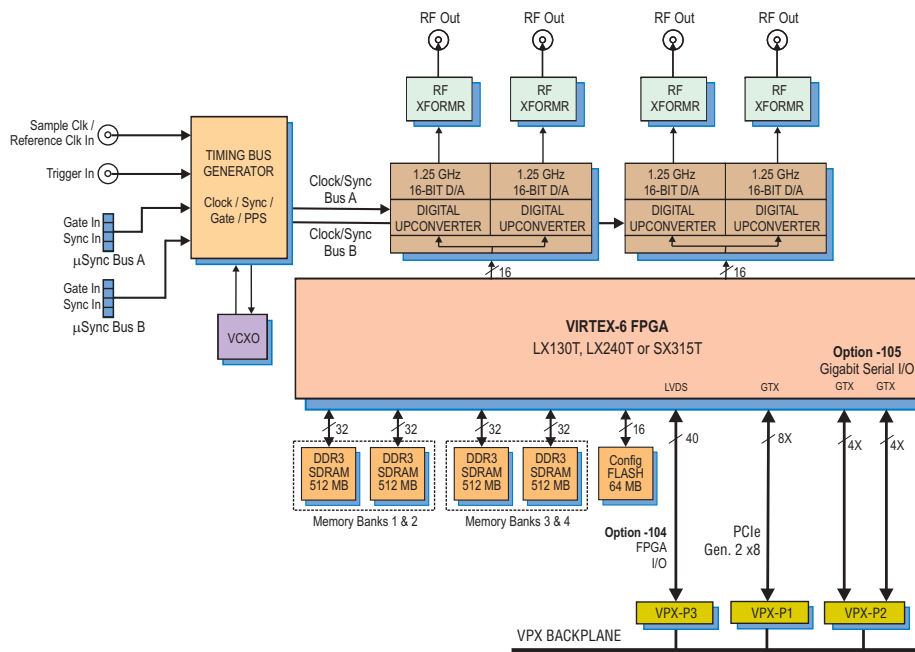
VITA 49.0 solves this problem by providing a framework for SDR receivers used for analysis of RF spectrum and localization of RF emissions. It is based upon a transport protocol layer to convey time-stamped digital data between components in the system. With a common protocol, SDR receivers can be interchanged, thereby enabling hardware upgrades and mitigating hardware lifecycle limitations. This eliminates the need to create new software to support each new receiver. The 53664 supports fully the VITA-49.0 specification.

Versions of the [53664](#) are also available as a different 3U VPX (Model [52664](#)), 6U VPX (Models [57664](#) and [58664](#) dual density), XMC (Model [71664](#)), x8 PCIe (Model [78664](#)), AMC (Model [56664](#)), 6U cPCI (Models [72664](#) and [74664](#) dual density), and 3U cPCI (Model [73664](#)).

Products

4-Channel 1.25 GHz D/A with DUC, Virtex-6 FPGA

Model 57670 - 6U VPX, Single Density



Model 57670
6U VPX
single density



Figure 63

Model 57670 is a member of the Cobalt family of high-performance 6U VPX boards based on the Xilinx Virtex-6 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications. It includes four D/As, four digital upconverters and four banks of memory. In addition to supporting PCI Express Gen. 2 as a native interface, the Model 57670 includes a front panel general-purpose connector for application-specific I/O.

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

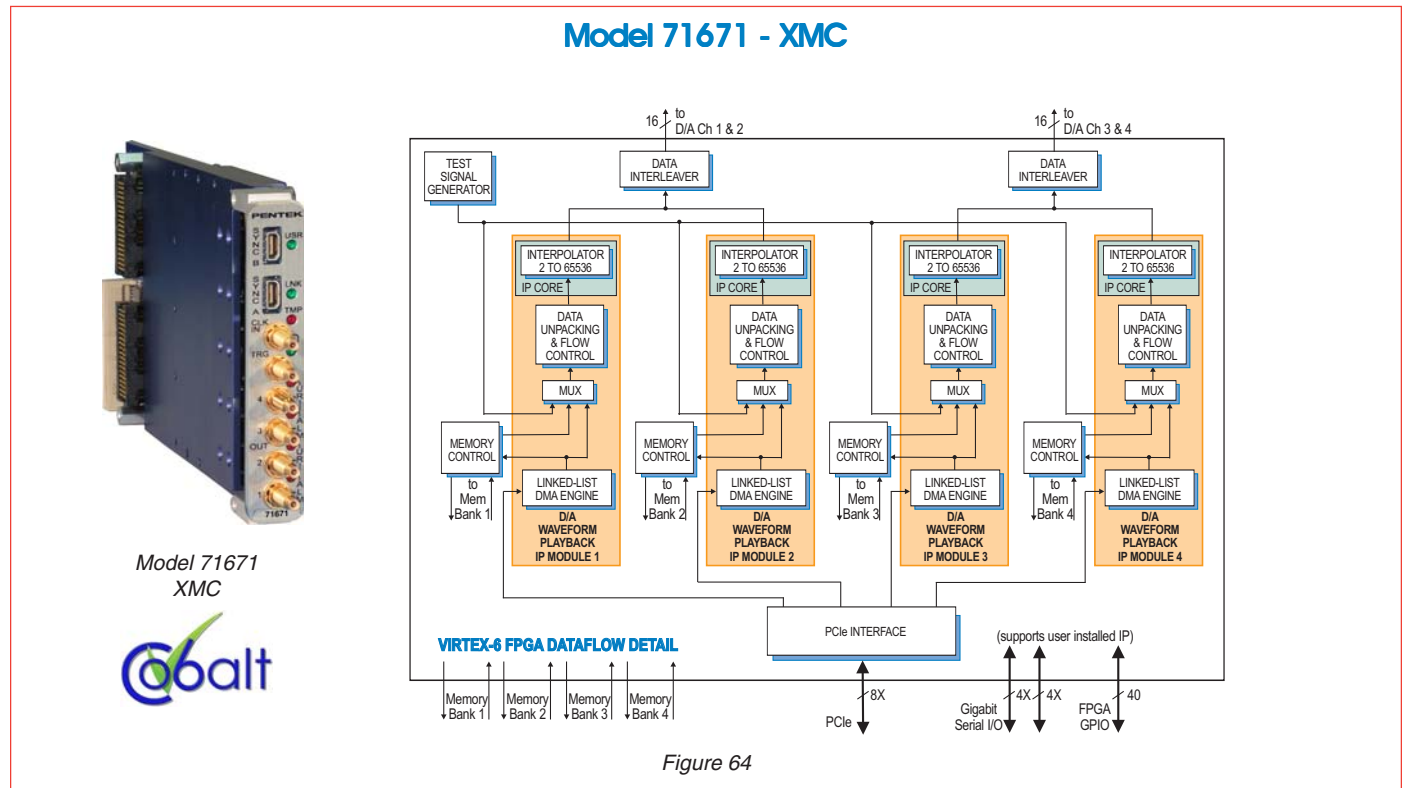
Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The Model 57670 factory-installed functions include a sophisticated D/A Waveform Playback IP module. Four linked-list controllers support waveform generation to the four D/As from tables stored in either on-board memory or off-board host memory.

IP modules for DDR3 SDRAM memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 57670 to operate as a turnkey solution without the need to develop FPGA IP.

Versions of the [57670](#) are also available as XMC (Model [71670](#)), x8 PCIe (Model [78670](#)), 3U VPX (Models [52670](#) and [53670](#)), 6U VPX (Model [58670](#) dual density), AMC (Model [56670](#)), 6U cPCI (Models [72670](#) and [74670](#) dual density), and 3U cPCI (Model [73670](#)).

Products

4-Channel 1.25 GHz D/A with DUC, Extended Interpolation, Virtex-6 FPGA



Model 71671 is a member of the Cobalt family of high-performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, high-speed data converter based on the Model 71670 described previously, it includes factory-installed IP cores to enhance the performance of the 71670 and address the requirements of many applications.

The Model 56671 factory-installed functions include a sophisticated D/A Waveform Playback IP module. Four linked-list controllers support waveform generation to the four D/As from tables stored in either on-board memory or off-board host memory.

Two Texas Instruments DAC3484s provide four DUC (digital upconverter) and D/A channels. Each channel accepts a baseband real or complex data stream from the FPGA and provides that input to the upconvert, interpolate and D/A stage.

When operating as a DUC, it interpolates and translates real or complex baseband input signals to a user

selectable IF center frequency. It delivers real or quadrature (I+Q) analog outputs to a 16-bit D/A converter.

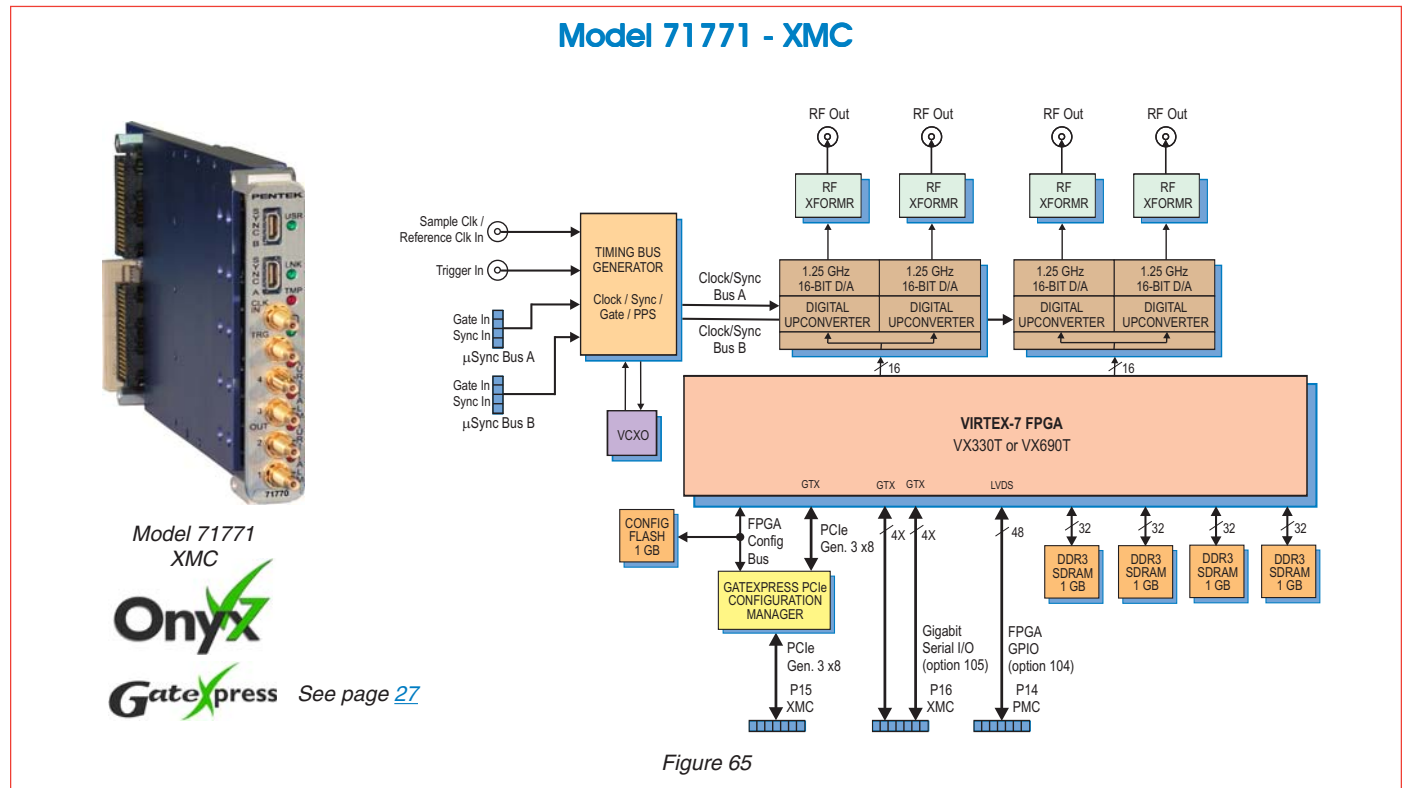
If translation is disabled, each D/A acts as an interpolating 16-bit D/A with output sampling rates up to 1.25 GHz. In both modes, the D/A provides interpolation factors of 2x, 4x, 8x and 16x.

In addition to the DAC3484, the 71671 features an FPGA-based interpolation engine which adds two additional interpolation stages programmable from 2x to 256x. The combined interpolation results in a range from 2x to 1,048,576x for each D/A channel and is ideal for matching the digital downconversion and data reduction used on the receiving channels of many communications systems.

Versions of the [71761](#) are also available as an x8 PCIe half-length board (Model [78671](#)), 3U VPX (Models [52671](#) and [53671](#)), 6U VPX (Models [57671](#) and [58671](#) with dual density), AMC (Model [56671](#)), 6U cPCI (Models [72671](#) and [74671](#) with dual density), and 3U cPCI (Model [73671](#)).

Products

4-Channel 1.25 GHz D/A with DUC, Extended Interpolation, Virtex-7 FPGA



Model 71771 is a member of the Onyx family of high-performance XMC modules based on the Xilinx Virtex-7 FPGA. This 4-channel, high-speed data converter is suitable for connection to transmit HF or IF ports of a communications or radar system. Its built-in data playback features offer an ideal turnkey solution for demanding transmit applications.

It includes four digital upconverters, four D/As with a wide range of programmable interpolation factors, and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71771 includes optional general-purpose and gigabit serial connectors for application-specific I/O.

The Pentek Onyx architecture features a Virtex-7 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control.

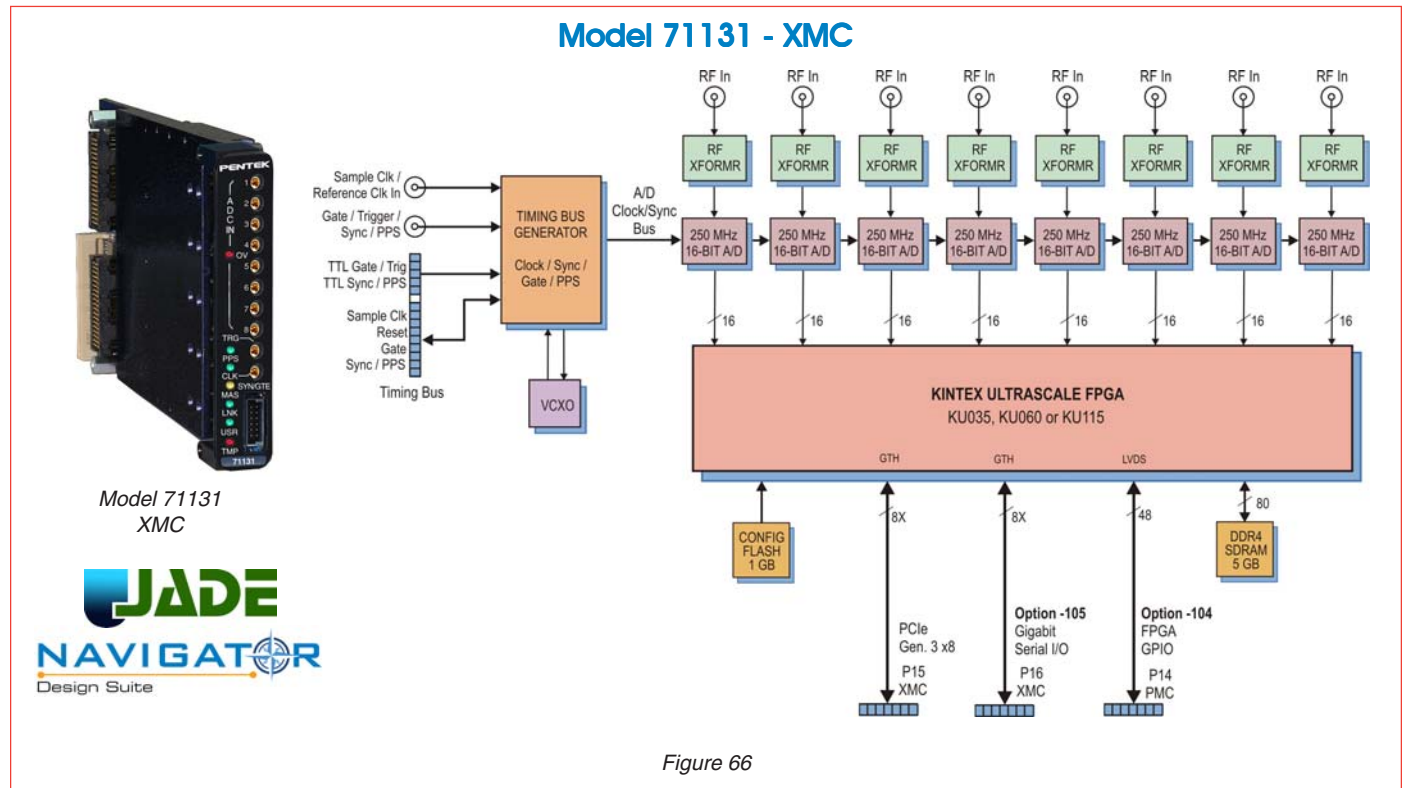
The Model 71771 factory-installed functions include a sophisticated D/A Waveform Playback IP module to support waveform generation to the four D/As from tables stored in on-board or off-board host memory.

Two Texas Instruments DAC3484s provide four DUC and D/A channels with interpolation factors of 2x, 4x, 8x and 16x. In addition to the DAC3484, the 71771 features an FPGA-based interpolation engine. The combined total interpolation results in a range from 2x to 1,048,576x for each D/A channel and is ideal for matching the digital downconversion and data reduction used on the receiving channels of many communications systems. See the block diagram of the 71671 on the previous page for more detail.

Versions of the [71771](#) are also available as an x8 PCIe half-length board (Model [78771](#)), 3U VPX (Models [52771](#) and [53771](#)), 6U VPX (Models [57771](#) and [58771](#) with dual density), AMC (Model [56771](#)), 6U cPCI (Models [72771](#) and [74771](#) with dual density), and 3U cPCI (Model [73771](#)).

Products

8-Channel 250 MHz A/D with DDCs, Kintex UltraScale FPGA



Model 71831 is a member of the Jade™ family of high-performance XMC modules. The Jade architecture embodies a new streamlined approach to FPGA-based boards, simplifying the design to reduce power and cost, while still providing some of the highest-performance FPGA resources available today. Designed to work with Pentek's new Navigator™ Design Suite of tools, the combination of Jade and Navigator offers users an efficient path to developing and deploying FPGA-based data acquisition and processing.

The 71131 is a multichannel, high-speed data converter with programmable DDCs. It is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture feature offers an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

It includes eight A/Ds, a complete multi-board clock and sync section and a large DDR4 memory. In addition to supporting PCI Express Gen. 3 as a native interface, the

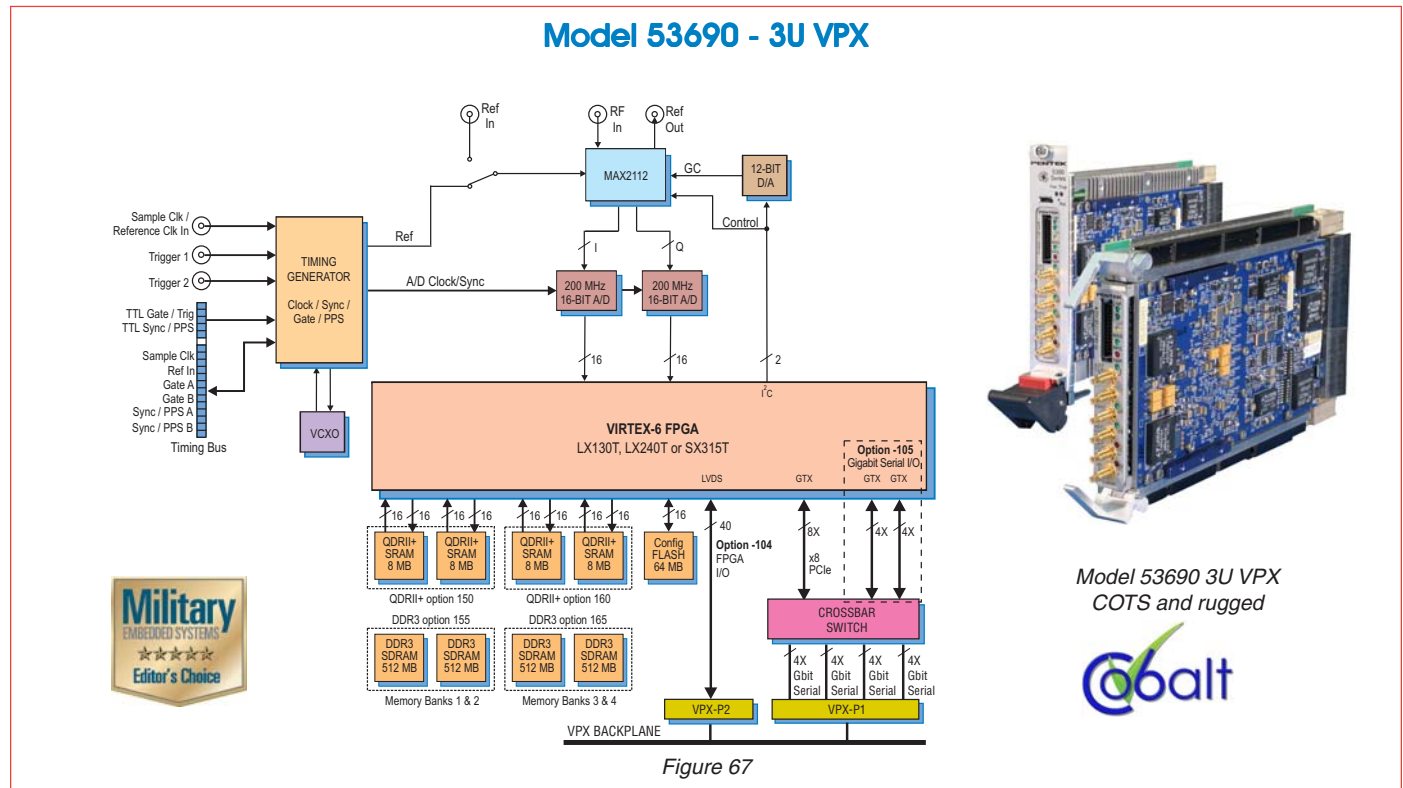
Model 71131 includes optional high-bandwidth connections to the Kintex UltraScale FPGA for custom digital I/O.

Each member of the Jade family is delivered with factory-installed applications ideally matched to the board's analog interfaces. The 71131 factory-installed functions include eight A/D acquisition IP modules for simplifying data capture and transfer. Each of the eight acquisition IP modules contains a powerful, programmable DDC IP core; an IP module for DDR4 SDRAM memory; a controller for all data clocking and synchronization functions; a test signal generator; and a PCIe interface. These complete the factory-installed functions and enable the 71131 to operate as a complete turnkey solution for many applications.

Versions of the [71131](#) are also available as an x8 PCIe half-length board (Model [78131](#)), 3U VPX (Models [52131](#) and [53131](#)), 6U VPX (Models [57131](#) and [58131](#) (dual density), AMC (Model [56131](#)), 6U cPCI (Models [72131](#) and [74131](#) with dual density), and 3U cPCI (Model [73131](#)).

Products

L-Band RF Tuner with 2-Channel 200 MHz A/D and Virtex-6 FPGA



Model 53690 is a member of the Cobalt family of high-performance 3U VPX boards based on the Xilinx Virtex-6 FPGA. A 2-channel high-speed data converter, it is suitable for connection directly to the RF port of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution. The Model 53690 includes an L-Band RF tuner, two 200 MHz, 16-bit A/Ds and four banks of memory. It features built-in support for PCI Express over the 3U VPX backplane.

The Pentek Cobalt architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data multiplexing, channel selection, data packing, gating, triggering and memory control. The Cobalt architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the

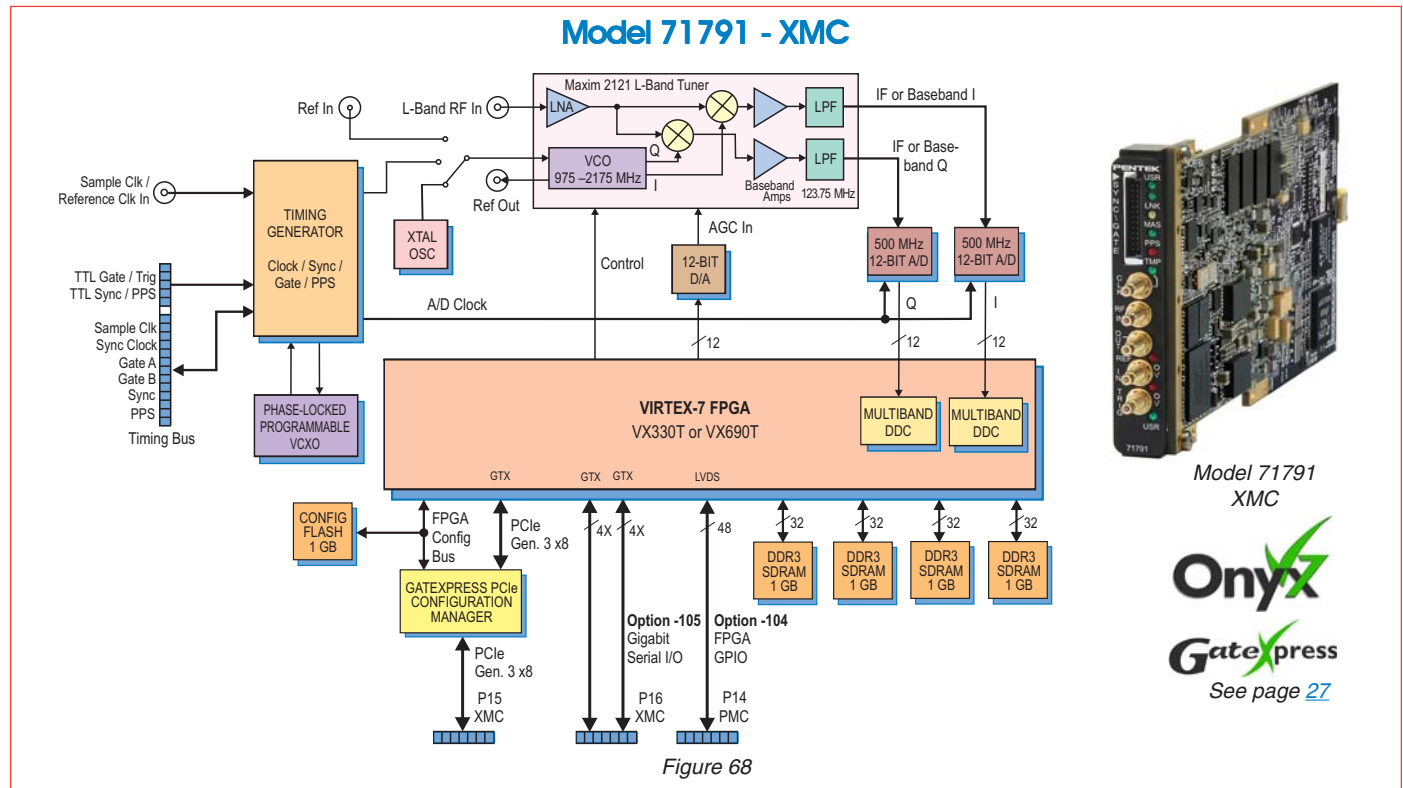
board's analog interfaces. The 53690 factory-installed functions include two A/D acquisition IP modules. IP modules for either DDR3 or QDRII+ memories, a controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions.

A front panel connector accepts L-Band signals between 925 MHz and 2175 MHz from an antenna LNB. A Maxim MAX2112 tuner directly converts these signals to baseband using a broadband I/Q downconverter. The device includes an RF variable-gain LNA (low-noise amplifier), a PLL synthesized local oscillator, quadrature (I + Q) down-converting mixers, baseband lowpass filters and variable-gain baseband amplifiers.

Versions of the [53690](#) are also available as an XMC (Model [71690](#)), an x8 PCI board (Model [78690](#)), 3U VPX (Model [52690](#)), 6U VPX (Models [57690](#) and [58690](#) dual density), AMC (Model [56690](#)), 6U cPCI (Models [72690](#) and [74690](#) dual density), and 3U cPCI (Model [73690](#)).

Products

L-Band RF Tuner with 2-Channel 500 MHz A/D and Virtex-7 FPGA



Model 71791 is a member of the Onyx family of high-performance XMC modules based on the Xilinx Virtex-7 FPGA. It is suitable for connection directly to an L-band signal for SATCOM and communications systems. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA processing IP.

It includes an L-Band RF tuner, two A/Ds and four banks of memory. In addition to supporting PCI Express Gen. 3 as a native interface, the Model 71791 includes general purpose and gigabit serial connectors for application-specific I/O.

The Pentek Onyx Architecture features a Virtex-7 FPGA. All of the board's data and control paths are accessible by the FPGA, to support factory-installed functions including data acquisition, control, channel selection, data packing, gating, triggering and memory control. The Onyx Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

The 71791 factory-installed functions include two A/D acquisition IP modules, four DDR3 memory controllers, two DDCs (digital downconverters), an RF tuner controller, a clock and synchronization generator, a test signal generator, and a Gen 3 PCIe interface.

A front panel SSMC connector accepts L-Band signals between 925 MHz and 2175 MHz, typically from an L-Band antenna or an LNB (low noise block). The Maxim MAX2121 tuner directly converts these L-Band signals to IF or baseband using a broadband I/Q downconverter. The device includes an RF variable-gain LNA, a PLL (phase-locked loop) synthesized local oscillator, quadrature (I+Q) down-converting mixers, output low pass filters, and variable-gain baseband amplifiers.

Versions of the [71791](#) are also available as an x8 PCIe half-length board (Model [78791](#)), 3U VPX (Models [52791](#) and [53791](#)), 6U VPX (Models [57791](#) and [58791](#) with dual density), AMC (Model [56791](#)), 6U cPCI (Models [72791](#) and [74791](#) with dual density), and 3U cPCI (Model [73791](#)).

Products

LVDS Digital I/O with Virtex-6 FPGA

Model 71610 - XMC

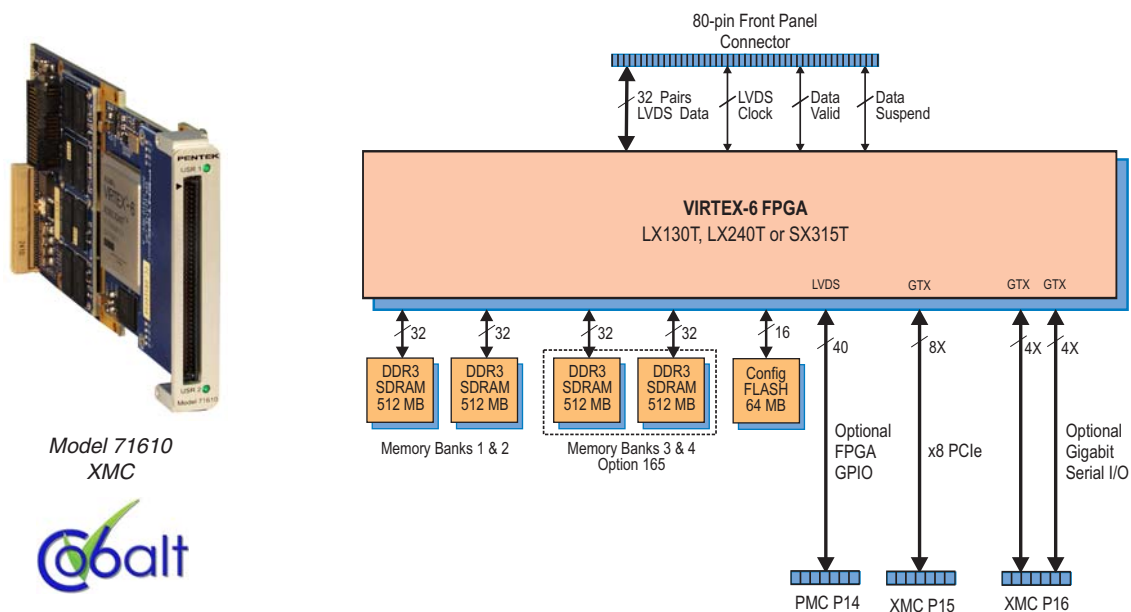


Figure 69

Model 71610 is a member of the Cobalt family of high-performance XMC modules based on the Xilinx Virtex-6 FPGA. This digital I/O module provides 32 LVDS differential inputs or outputs plus LVDS clock, data valid, and data flow control on a front panel 80-pin connector. Its built-in data capture and data generation feature offers an ideal turnkey solution.

In addition to supporting PCI Express as a native interface, the Model 71610 includes a general-purpose connector for application-specific I/O.

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data transfer and memory control. The Cobalt Architecture organizes the FPGA as a container for data processing applications where each function exists as an intellectual property (IP) module.

Each member of the Cobalt family is delivered with factory-installed applications ideally matched to the

board's interface. The 71610 factory-installed functions include 32-bit acquisition and generation IP modules, to support either input or output functions, respectively.

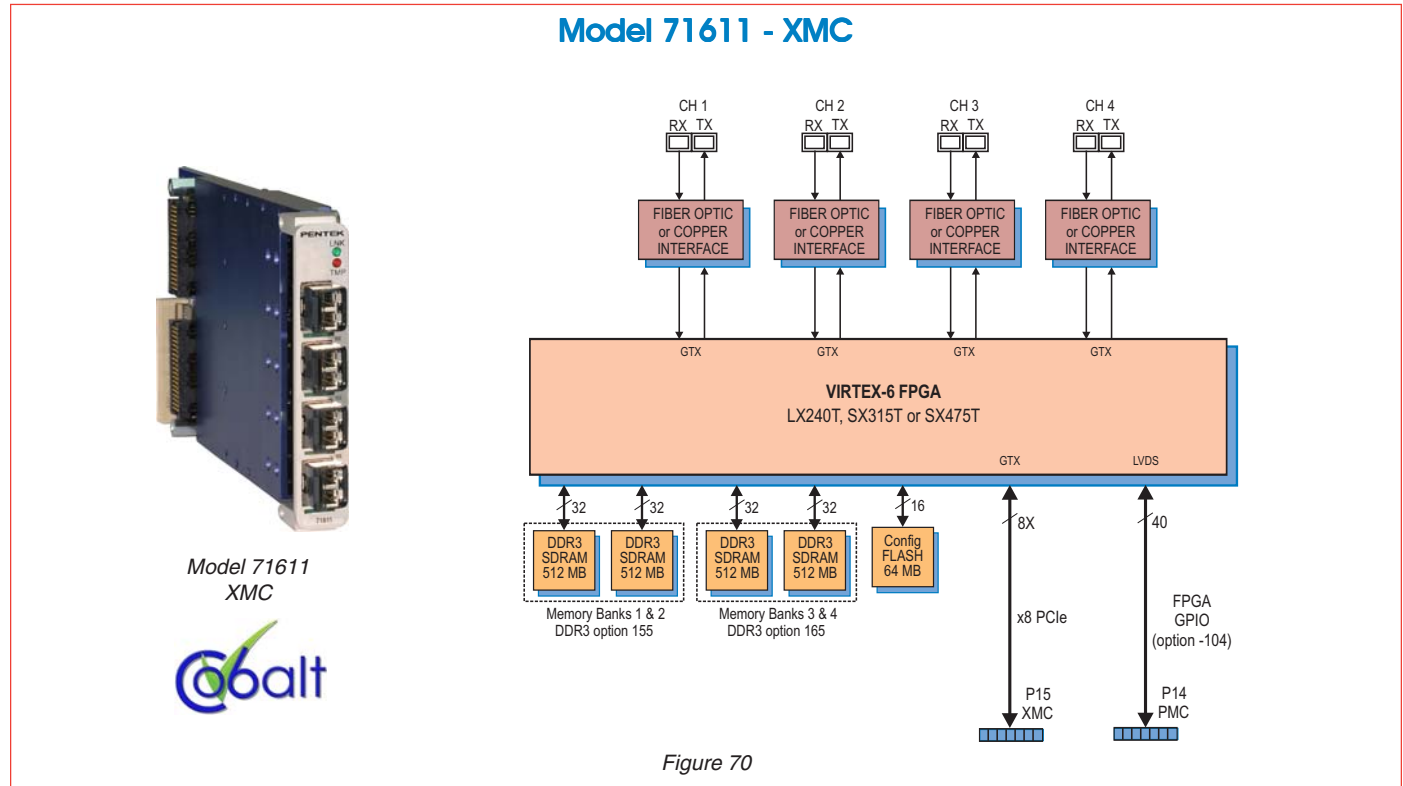
IP modules for DDR3 SDRAM memories, a controller for all data clocking, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 71610 to operate as a complete turnkey solution without the need to develop any FPGA IP.

The Model 71610 includes an industry-standard interface fully compliant with PCI Express Gen. 1 bus specifications. Supporting a PCIe x4 or x8 connection, the interface includes multiple DMA controllers for efficient transfers to and from the module.

Versions of the [71610](#) are also available as an x8 PCIe board (Model [78610](#)), 3U VPX (Models [52610](#) and [53610](#)), 6U VPX (Models [57610](#) and [58610](#) dual density), AMC (Model [56610](#)), 6U cPCI (Models [72610](#) and [74610](#) with dual density), and 3U cPCI (Model [73610](#)).

Products

Digital I/O: Quad Serial FPDP Interface with Virtex-6 FPGA



Model 71611 is a member of the Cobalt family of high-performance XMC modules based on the Xilinx Virtex-6 FPGA. A multichannel, gigabit serial interface, it is ideal for interfacing to serial FPDP data converter boards or as a chassis-to-chassis data link.

The 71611 is fully compatible with the VITA 17.1 Serial FPDP specification. Its built-in data transfer features make it a complete turnkey solution. For users who require application-specific functions, the 71611 serves as a flexible platform for developing and deploying custom FPGA processing IP.

In addition to supporting PCI Express as a native interface, the Model 71611 includes a general purpose connector for application-specific I/O.

The Pentek Cobalt Architecture features a Virtex-6 FPGA. All of the board's data and control paths are accessible by the FPGA, enabling factory-installed functions including data transfer and memory control. The Cobalt Architecture organizes the FPGA as a container

for data processing applications where each function exists as an intellectual property (IP) module.

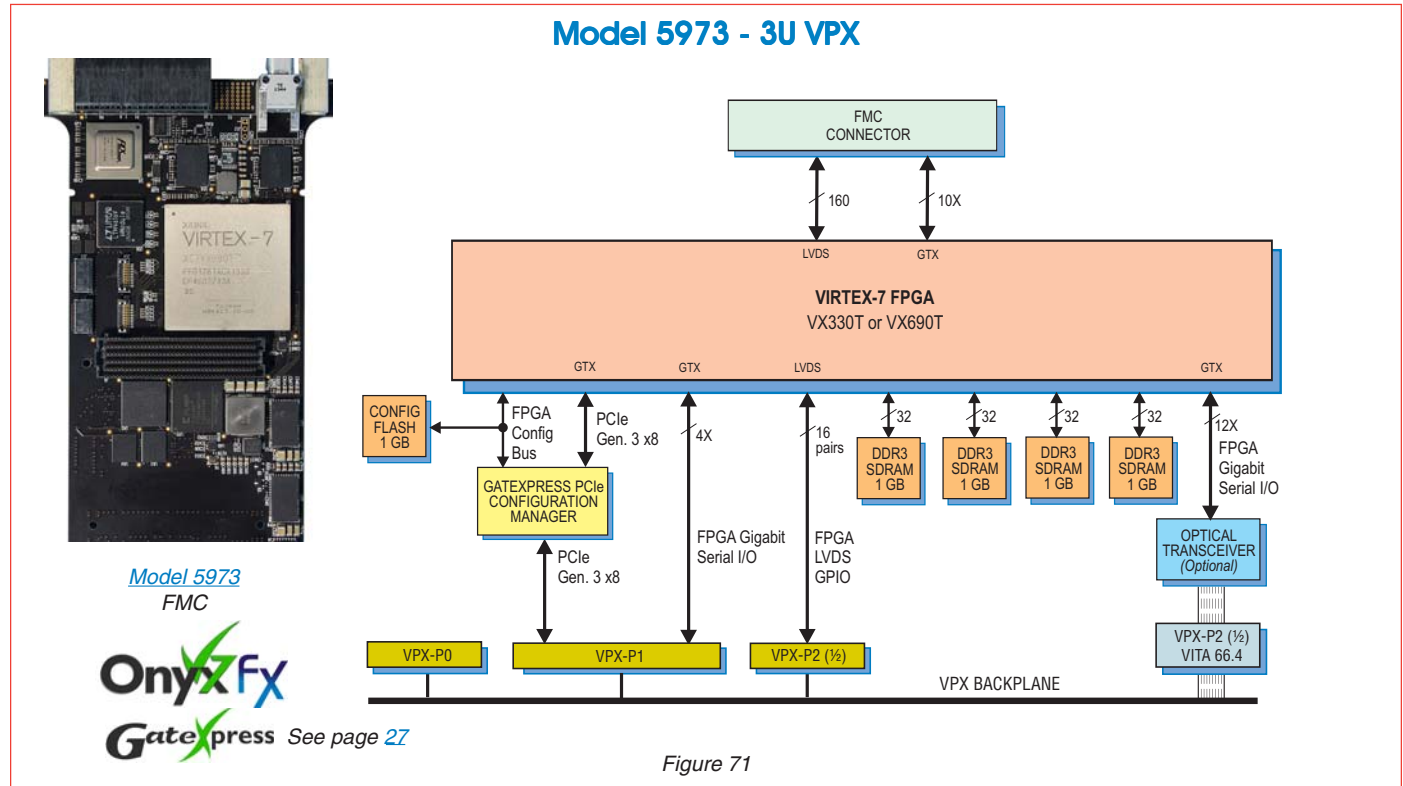
IP modules for DDR3 SDRAM memories, controllers for data routing and flow control, CRC support, advanced DMA engines, and a PCIe interface complete the factory-installed functions and enable the 71611 to operate as a complete turnkey solution without developing FPGA IP.

The 71611 is fully compatible with the VITA 17.1 Serial FPDP specification. With the capability to support 1.0625, 2.125, 2.5, 3.125, and 4.25 Gbaud link rates and the option for multi-mode and single-mode optical interfaces, the board can work in virtually any system. Programmable modes include: flow control in both receive and transmit directions, CRC support, and copy/loop.

Versions of the [71611](#) are also available as an x8 PCIe board (Model [78611](#)), 3U VPX (Models [52611](#) and [53611](#)), 6U VPX (Models [57611](#) and [58611](#) dual density), AMC (Model [56611](#)), 6U cPCI (Models [72611](#) and [74611](#) with dual density), and 3U cPCI (Model [73611](#)).

Products

Virtex-7 Processor and FMC Carrier - FMC



The OnyxFX™ Model 5973 is a high-performance 3U VPX board based on the Xilinx Virtex-7 FPGA. As a stand-alone processor board, it provides an ideal development and deployment platform for demanding signal-processing applications.

The 5973 includes a VITA-57.1 FMC site providing access to a wide range of Flexor® I/O options. When combined with any of Pentek's analog interface FMCs, it becomes a complete multichannel data conversion and processing subsystem suitable for connection to IF, HF or RF ports of a communications or radar system.

The 5973 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on an MTP connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 5973s mounted in the same chassis or even over extended distances between them.

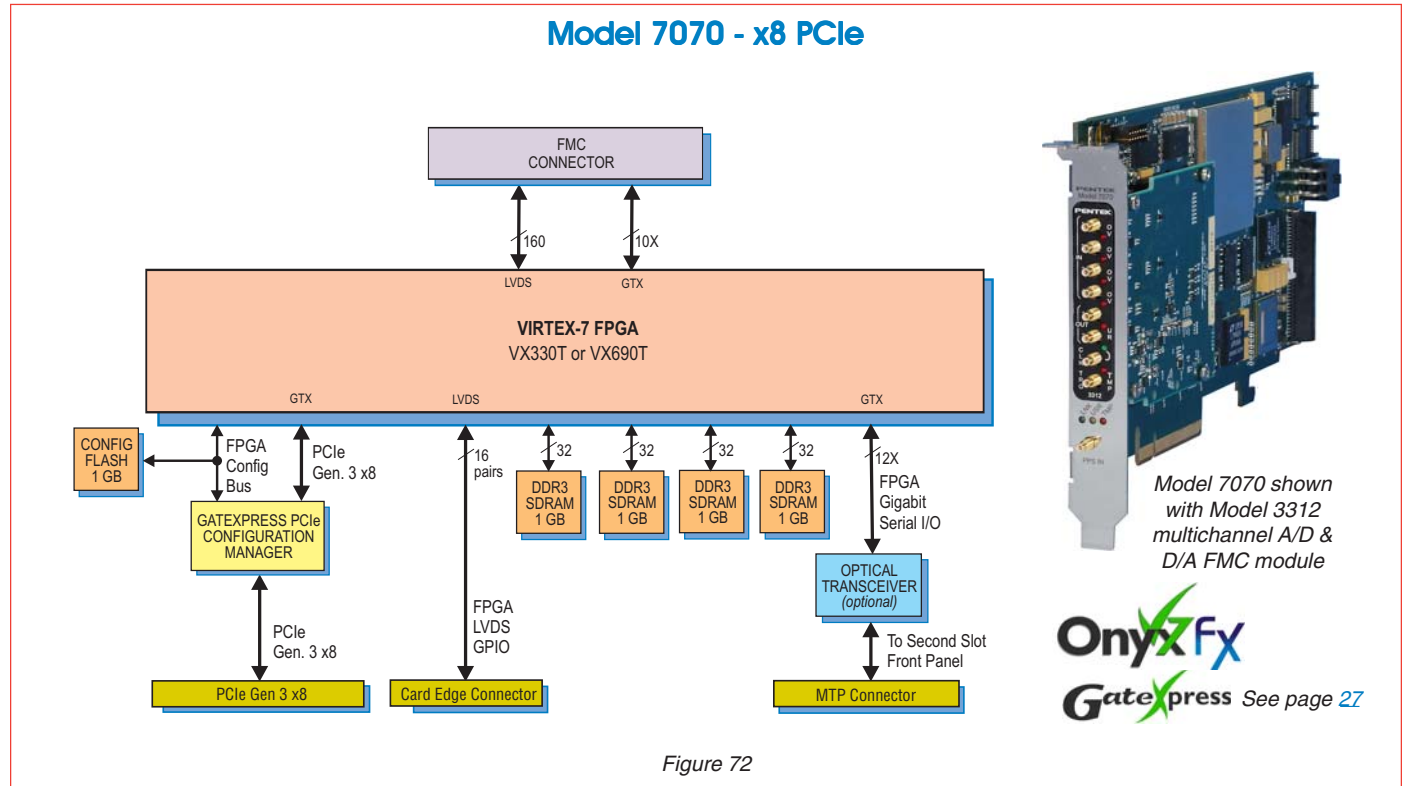
When integrated with a Pentek FMC, the 5973 is delivered with factory-installed applications ideally matched to the board's analog or digital interfaces. These can include A/D acquisition and D/A waveform playback engines for simplifying data capture and playback.

Data tagging and metadata packet generation, in conjunction with powerful linked-list DMA engines, provide a streamlined interface for moving data on and off the board and identifying data packets with channel, timing and sample count information.

IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the 5973 and its installed FMC to operate as a complete turnkey solution without the need to develop any FPGA IP.

Products

PCI Express Virtex-7 Processor and FMC Carrier - FMC



The OnyxFX Model [7070](#) is a high-performance PCIe board based on the Xilinx Virtex-7 FPGA. As a stand-alone processor board, it provides an ideal development and deployment platform for demanding signal processing applications.

The 7070 includes a VITA-57.1 FMC site providing access to a wide range of Flexor I/O options. When combined with any of Pentek's analog interface FMCs, it becomes a complete multichannel data conversion and processing subsystem suitable for connection to IF, HF or RF ports of a communications or radar system.

The 7070 architecture includes an optional built-in gigabit serial optical interface. Up to 12 high-speed duplex optical lanes are available on an MTP connector. With the installation of a serial protocol in the FPGA, this interface enables a high-bandwidth connection between 7070s mounted in the same chassis or even over extended distances between them.

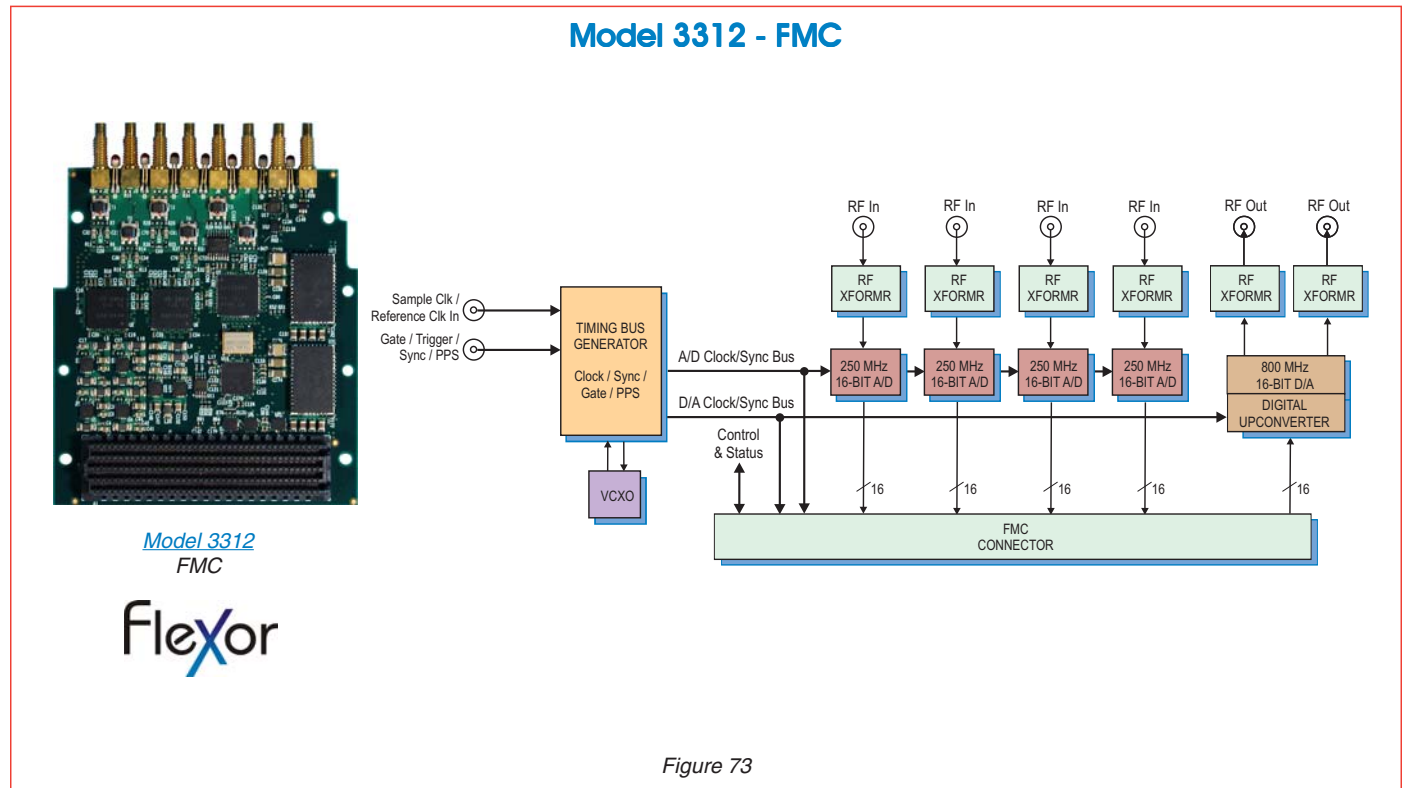
When integrated with a Pentek FMC, the 7070 is delivered with factory-installed applications ideally matched to the board's analog or digital interfaces. These can include A/D acquisition and D/A waveform playback engines for simplifying data capture and playback.

Data tagging and metadata packet generation, in conjunction with powerful linked-list DMA engines, provide a streamlined interface for moving data on and off the board and identifying data packets with channel, timing and sample-count information.

IP modules for DDR3 SDRAM memories, controllers for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable the [7070](#) and installed FMC to operate as a complete turnkey solution without the need to develop any FPGA IP.

Products

4-Channel 250 MHz 16-bit A/D, 2-Channel 800 MHz 16-bit D/A



The Flexor [Model 3312](#) is a multichannel, high-speed data converter FMC module. It is suitable for connection to HF or IF ports of a communications or radar system. It includes four 250 MHz, 16-bit A/Ds, two 800 MHz, 16-bit D/As, programmable clocking, and multiboard synchronization for support of larger high-channel-count systems.

When combined with either the Model 5973 3U VPX or Model 7070 PCIe FMC carrier, the board-set becomes a turnkey data acquisition and signal generation solution. For applications that require custom processing, the board-set is an ideal IP development and deployment subsystem.

The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into two Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

While users will find the [Model 3312](#) an excellent analog interface to any compatible FMC carrier, the true performance of the 3312 can be unlocked only when used with the Pentek Model 5973 or Model 7070 FMC carriers.

With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and a D/A waveform playback IP module.

When used with the 5973 or the 7070, the [3312](#) features a sophisticated D/A waveform playback IP module. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory.

Products

4-Channel 250 MHz A/D, 2-Channel 800 MHz D/A

3U VPX FlexorSet 5973-312 or x8 PCIe FlexorSet 7070-312

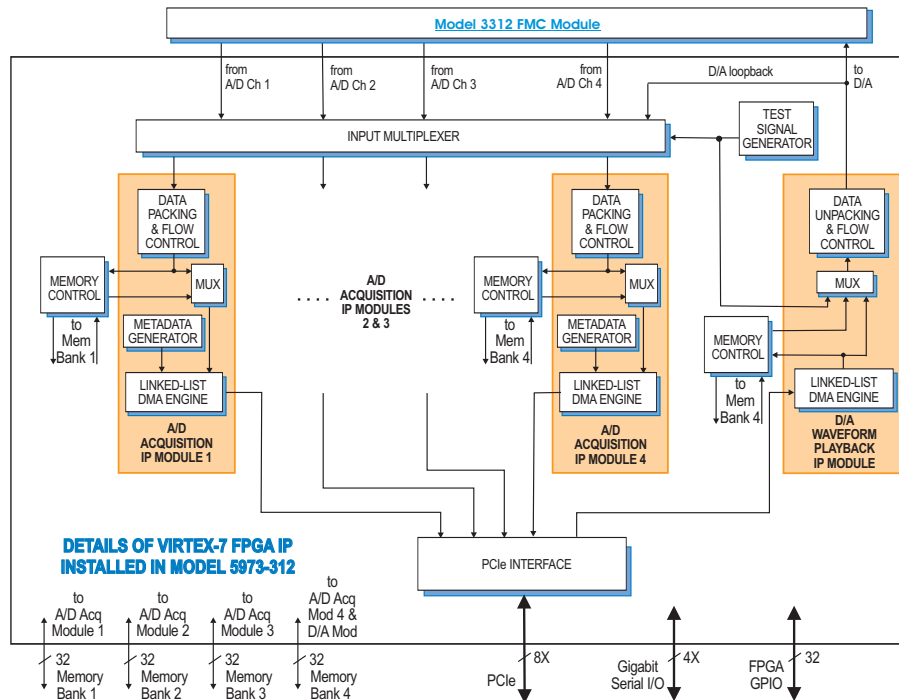


Figure 74



Model 5973-312

GateFlow
ReadyFlow
 Board Support Package

OnyxFx
GateXpress See page 27

Models [5973-312](#) and [7070-312](#) are members of the FlexorSet™ family of high-performance 3U VPX or x8 PCIe boards based on the Xilinx Virtex-7 FPGA.

As FlexorSet integrated solutions, the Model 3312 FMC is factory-installed on the 5973 or 7070 carrier. The required FPGA IP is installed and the board set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

Each FlexorSet includes four 250 MHz, 16-bit A/Ds, one digital upconverter, two 800 MHz, 16-bit D/As, and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, these models include optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

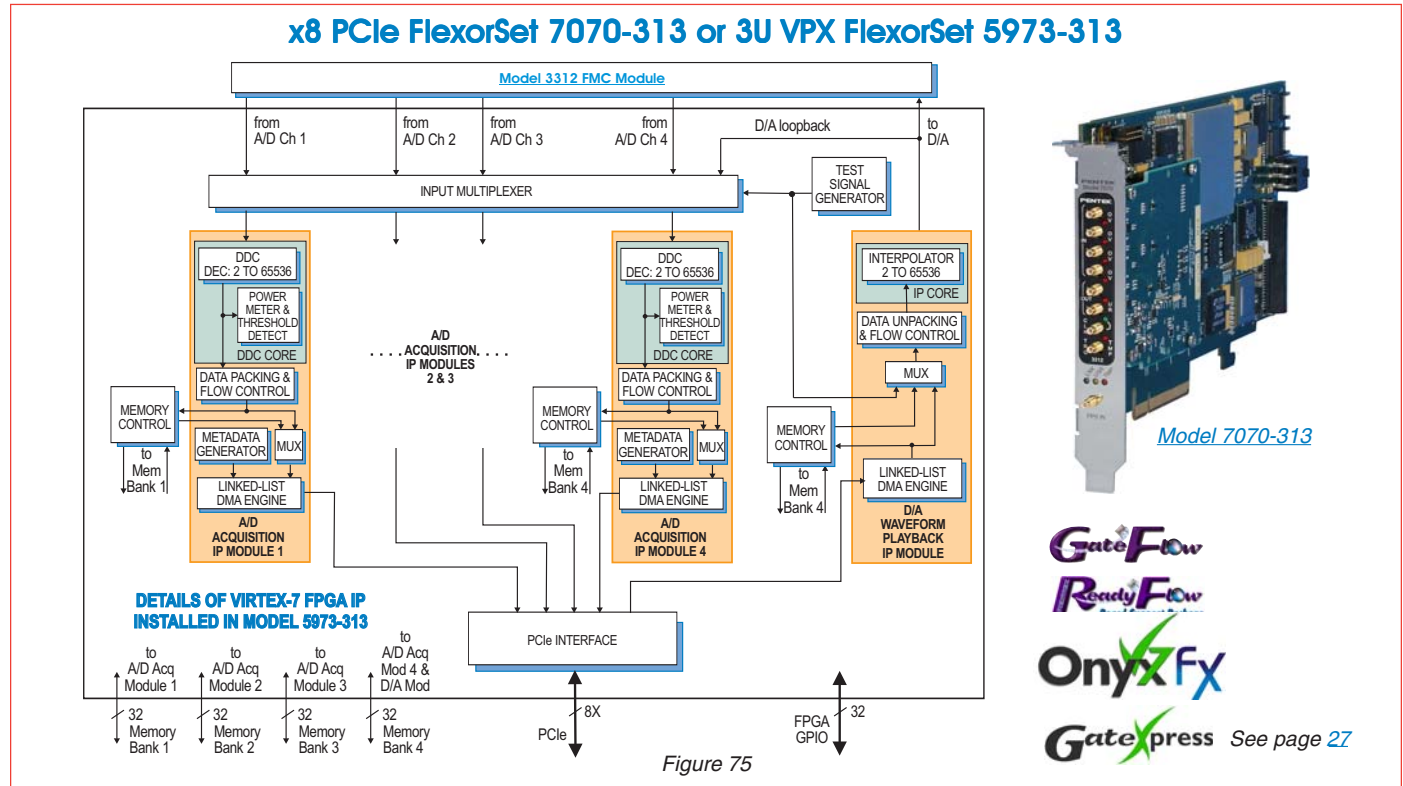
When delivered as an assembled board set, the FlexorSet includes factory-installed applications ideally matched to the board's analog interfaces. The functions include four A/D acquisition IP modules for simplifying data capture and data transfer. Each of the four acquisition IP modules contains IP modules for DDR3 SDRAM memories.

Both models feature a sophisticated D/A waveform playback IP module. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. Up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as turnkey solutions without the need to develop any FPGA IP.

Products

4-Channel 250 MHz A/D with DDCs, 2-Channel 800 MHz D/A with Extended Interpolation



Models [7070-313](#) and [5973-313](#) are members of the FlexorSet family of high-performance x8 PCIe or 3 U VPX boards based on the Xilinx Virtex-7 FPGA.

As FlexorSet integrated solutions, the Model 3312 FMC is factory-installed on the 7070 or 5973 carrier. The required FPGA IP is installed and the board-set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs and is suitable for connection to HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

Each FlexorSet includes four 250 MHz, 16-bit A/Ds, one digital upconverter, two 800 MHz, 16-bit D/As, and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, these models include optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

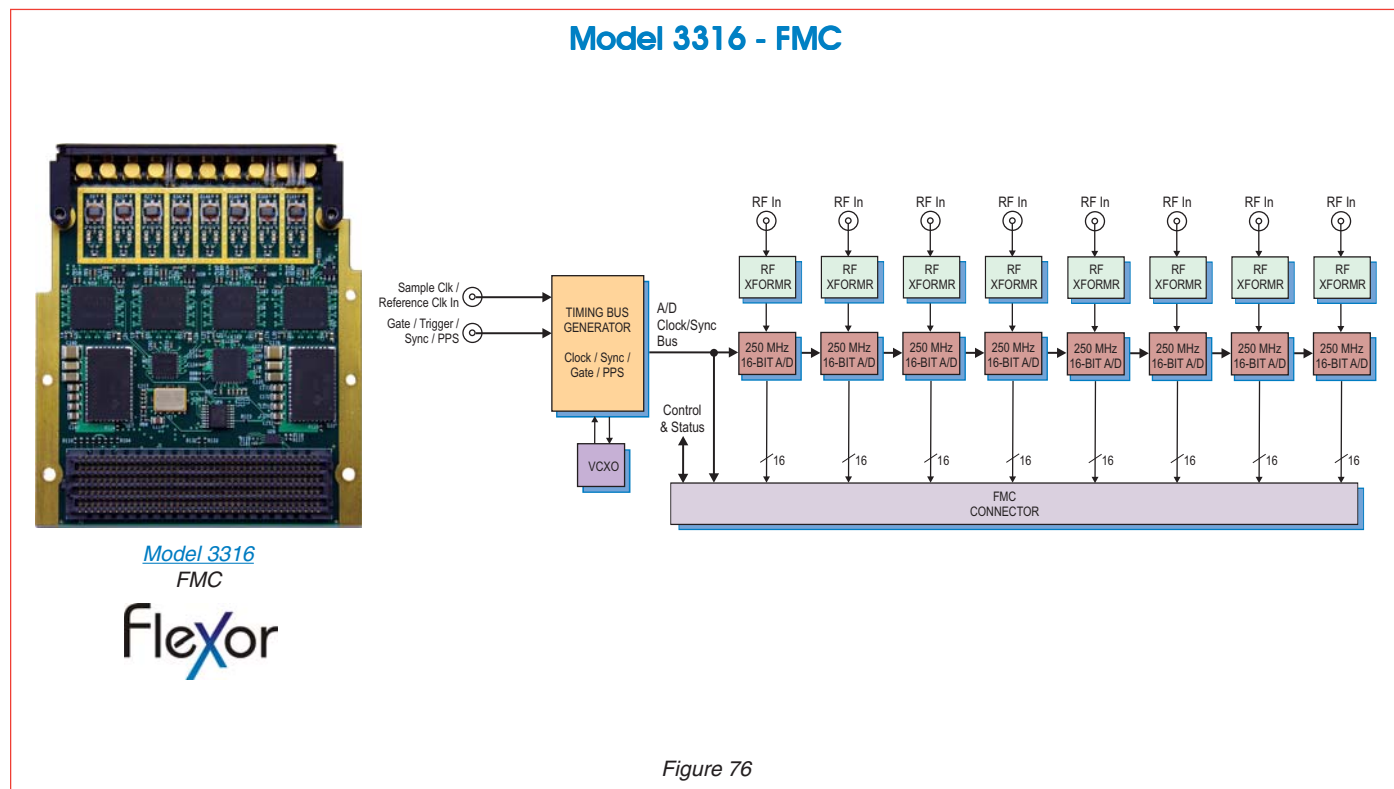
When delivered as an assembled board-set, the FlexorSet includes factory-installed applications ideally matched to the board's analog interfaces. The functions include four A/D acquisition IP modules for simplifying data capture and data transfer. Each of the four acquisition IP modules contains a programmable DDC core with decimations from 2 to 65,536.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB. Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q or 16-bit I + 16-bit Q samples at a rate of f_s / N .

A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as turnkey solutions without the need to develop any FPGA IP.

Products

8-Channel 250 MHz 16-bit A/D



The Flexor [Model 3316](#) is a multichannel, high-speed data converter FMC module. It is suitable for connection to HF or IF ports of a communications or radar system. It includes eight 250 MHz, 16-bit A/Ds, on-board programmable clocking, and multiboard synchronization for support of larger high-channel-count systems.

When combined with either the Model 5973 3U VPX or Model 7070 PCIe carrier, the board-set becomes a turnkey data acquisition solution. For applications that require custom processing, the board-set is an ideal IP development and deployment subsystem.

The front end accepts eight analog HF or IF inputs on front-panel connectors with transformer-coupling into four Texas Instruments ADS42LB69 Dual 250 MHz, 16-bit A/D converters.

While users will find the Model 3316 an excellent analog interface to any compatible FMC carrier, the true performance of the 3316 can be unlocked only when used with the Pentek Model 5973 or Model 7070 carriers.

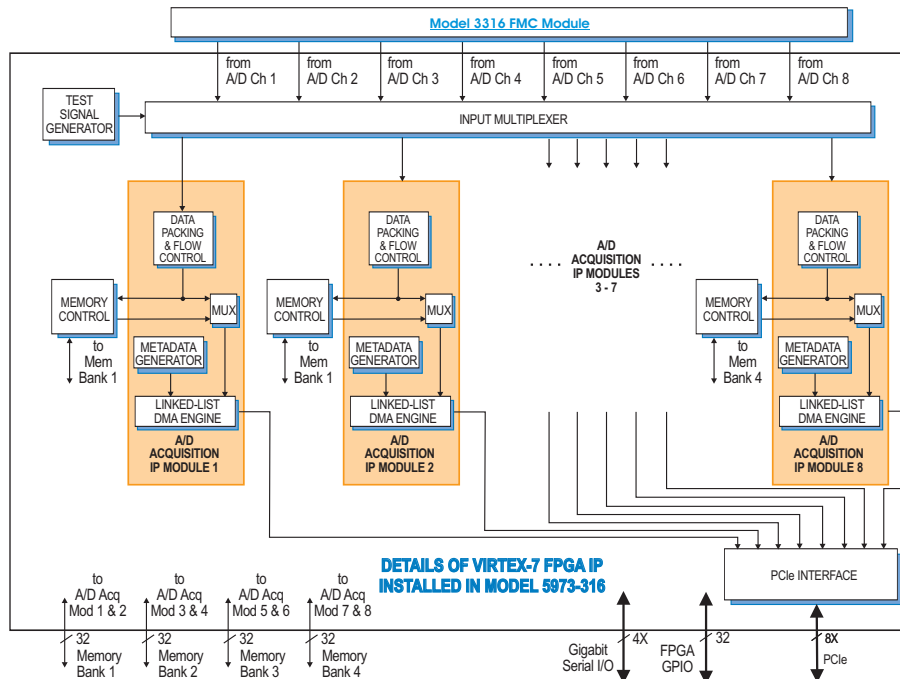
With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and a metadata packet creator.

When the [3316](#) is installed on either the 5973 or the 7070 FMC carrier, the board-set features eight A/D Acquisition IP modules for easily capturing and moving data. Each module can receive data from any of the eight A/Ds, or a test signal generator.

Products

8-Channel 250 MHz A/D with Virtex-7 FPGA - 3U VPX

3U VPX FlexorSet 5973-316 or x8 PCIe FlexorSet 7070-316



GateFlow

ReadyFlow

Board Support Package

Onyx7Fx

Gatepress

See page 27

Figure 77

Models [5973-316](#) and [7070-316](#) are members of the FlexorSet family of high-performance 3U VPX or x8 PCIe boards based on the Xilinx Virtex-7 FPGA.

As FlexorSet integrated solutions, the Model 3316 FMC is factory-installed on the 5973 or 7070 carrier. The required FPGA IP is installed and the board-set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

Each FlexorSet includes eight A/Ds and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, these models include optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

When delivered as an assembled board-set, the FlexorSet includes factory-installed applications ideally matched to the board's analog interfaces. These functions include eight A/D acquisition IP modules for simplifying data capture and transfer.

Each of the eight acquisition IP modules contains IP modules for DDR3 SDRAM memories. A controller for all data clocking and synchronization functions, a test signal generator, and a PCIe interface complete the factory-installed functions and enable these models to operate as turnkey solutions without the need to develop any FPGA IP.

For applications that require specialized functions, users can install their own custom IP for data processing. Pentek GateFlow FPGA Design Kits include all of the factory-installed modules as documented source code. Developers can integrate their own IP with the Pentek factory-installed functions or use the GateFlow kit to completely replace the Pentek IP with their own.

Products

8-Channel 250 MHz A/D with Digital Downconverters - x8 PCIe

x8 PCIe FlexorSet 7070-317 or 3U VPX FlexorSet 5973-317

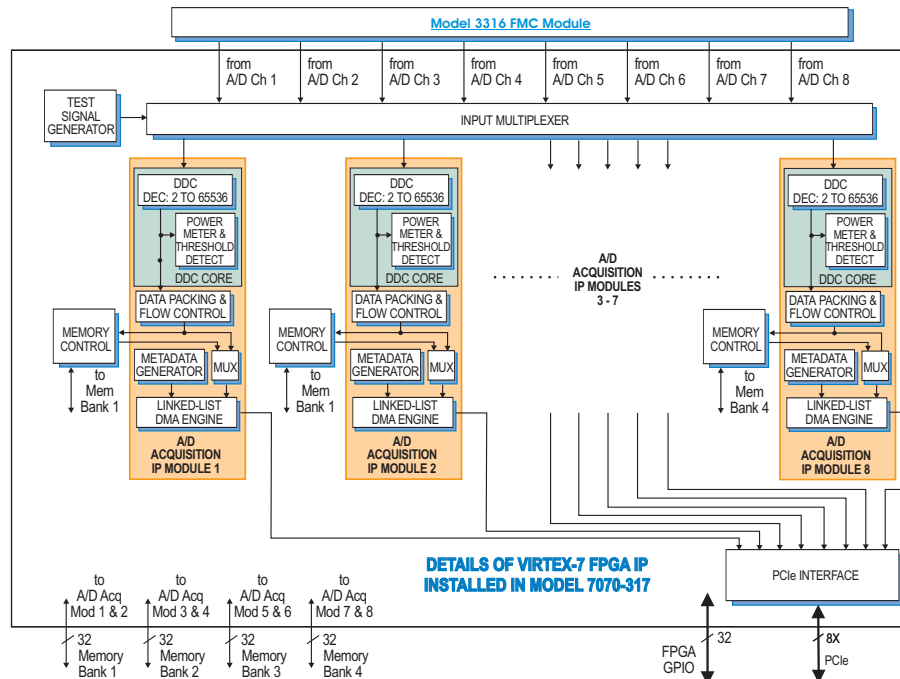


Figure 78



Model 7070-317

GateFlow
ReadyFlow
Based Connect Backdoor

OnyxFX

Gatepress See page 27

Models [7070-317](#) and [5973-317](#) are members of the FlexorSet family of high-performance x8 PCIe or 3U VPX boards based on the Xilinx Virtex-7 FPGA.

As FlexorSet integrated solutions, the Model 3316 FMC is factory-installed on the 7070 or 5973 carrier. The required FPGA IP is installed and the board-set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter with programmable DDCs (Digital Downconverters) and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

Each FlexorSet includes eight A/Ds and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, these models include optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

When delivered as an assembled board-set, the FlexorSet includes factory-installed applications ideally matched to the board's analog interfaces. The functions include eight A/D acquisition IP modules for simplifying data capture and data transfer.

Within each A/D Acquisition IP Module is a powerful DDC IP core. Each DDC has an independent 32-bit tuning frequency setting that ranges from DC to f_s , where f_s is the A/D sampling frequency. Each DDC can have its own unique decimation setting, supporting as many as eight different output bandwidths for the board. Decimations can be programmed from 2 to 65,536 providing a wide range to satisfy most applications.

The decimating filter for each DDC accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Products

2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A - FMC

Model 3320 - FMC

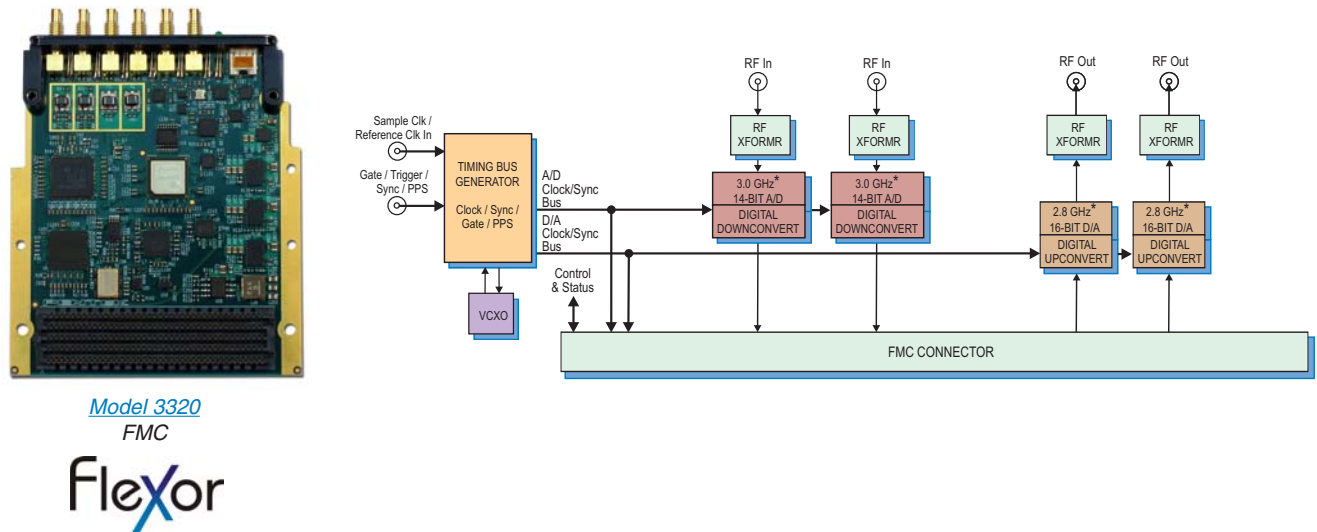


Figure 79

The Flexor [Model 3320](#) is a multichannel, high-speed data converter FMC. It is suitable for connection to RF or IF ports of a communications or radar system. It includes two 3.0 GHz A/Ds, two 2.8 GHz D/As, programmable clocking and multiboard synchronization for support of larger high-channel-count systems.

When combined with either the Model 5973 3U VPX or Model 7070 PCIe carrier, the board-set becomes a turnkey data acquisition solution. For applications that require custom processing, the board-set is an ideal IP development and deployment subsystem.

The true performance of the 3320 can be unlocked only when used with the Pentek Model 5973 or Model 7070 FMC carriers. With factory-installed IP, the board-set provides a turnkey data acquisition subsystem eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition, programmable linked-list DMA engines, and D/A waveform playback IP modules.

Designed to allow users to optimize data conversion rates and modes for specific application requirements, the FlexorSet provides preconfigured conversion profiles. Users can use these profiles which include: digital down-converter and digital upconverter modes, conversion resolution and A/D and D/A sample rates, or program their own profiles. In addition to supporting PCIe Gen. 3 as a native interface, the FlexorSet includes optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

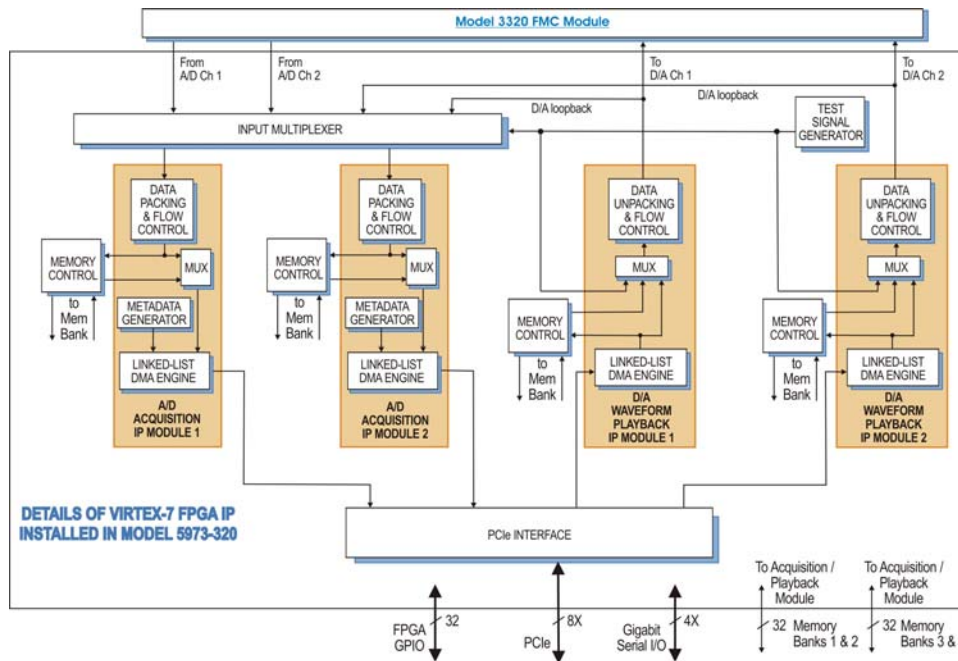
The front end accepts two analog RF or IF inputs on front-panel connectors with transformer-coupling into a Texas Instruments ADC32RF45 dual channel A/D. With dual built-in digital downconverters and programmable decimations, the converter serves as an ideal interface for a range of radar, signal intelligence and electronic counter-measures applications.

With the [3320](#) installed on either the 5973 or the 7070 carrier, the board-set features two A/D Acquisition IP modules for easily capturing and moving data.

Products

2-Channel 3.0 GHz A/D, 2-Channel 2.8 GHz D/A - FMC

3U VPX FlexorSet 5973-320 or x8 PCIe FlexorSet 7070-320



GateFlow
 ReadyFlow
 Board Support Package
 OnyxFx
 GateXpress
 See page 27

Figure 80

Models [5973-320](#) and [7070-320](#) are members of the FlexorSet family of high-performance 3U VPX or x8 PCIe boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet integrated solution, the Model 3320 FMC is factory-installed on the 5973 or 7070 carrier. The required FPGA IP is installed and the board-set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the RF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA- processing IP.

Designed to allow users to optimize data conversion rates and modes for specific application requirements, the FlexorSet provides preconfigured conversion profiles. Users can use these profiles which include: digital downconverter and digital upconverter modes, conversion resolution and A/D

and D/A sample rates, or program their own profiles. In addition to supporting PCIe Gen. 3 as a native interface, these models include optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

When delivered as an assembled board-set, these models include factory-installed applications ideally matched to the board's analog interfaces. The functions include two A/D acquisition IP modules for simplifying data capture and data transfer.

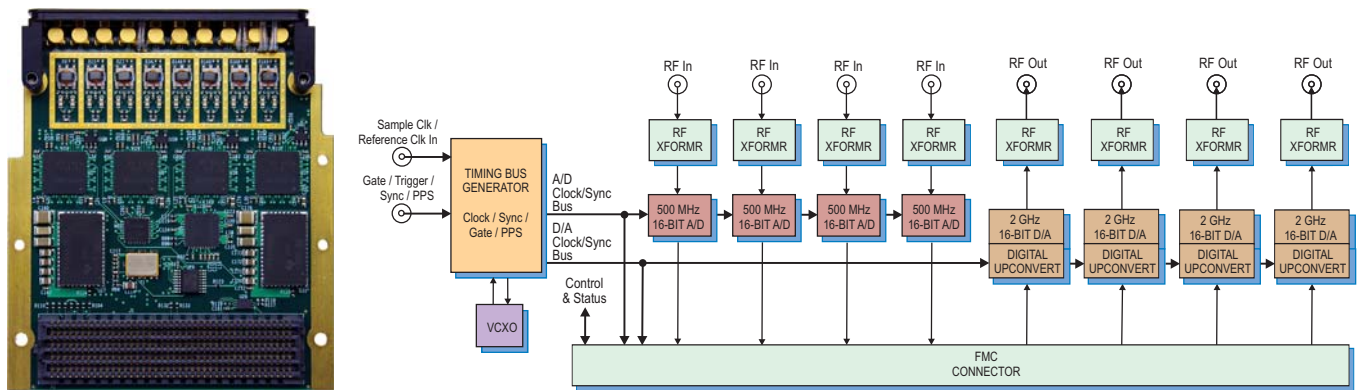
Each of the acquisition IP modules contains IP modules for DDR3 SDRAM memories.

Both FlexorSets feature two sophisticated D/A wave-form playback IP modules. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform.

Products

4-Channel 500 MHz 16-bit A/D, 4-Channel 2 GHz 16-bit D/A

Model 3324 - FMC



Model 3324
FMC
Flexor

Figure 81

The Flexor [Model 3324](#) is a multichannel, high-speed data converter FMC. It is suitable for connection to HF or IF ports of a communications or radar system. It includes four 500 MHz, 16-bit A/Ds, four 2 GHz, 16-bit D/As, programmable clocking, and multi-board synchronization for support of larger high-channel-count systems.

When combined with either the Model 5973 3U VPX or Model 7070 PCIe FMC carrier, the board-set becomes a turnkey data acquisition solution. For applications that require custom processing, the board-set is an ideal IP development and deployment subsystem.

The front end accepts four analog HF or IF inputs on front-panel connectors with transformer-coupling into four 500 MHz, 16-bit A/D converters.

While users will find the [Model 3324](#) an excellent analog interface to any compatible FMC carrier, the true

performance of the 3324 can be unlocked only when used with the Pentek Model 5973 or Model 7070 carriers.

With factory-installed IP, the board-set provides a turnkey data acquisition and signal generation subsystem, eliminating the need to create any FPGA IP. Installed features include flexible A/D acquisition engines, D/A waveform playback engines, programmable linked-list DMA engines, and a metadata-packet creator.

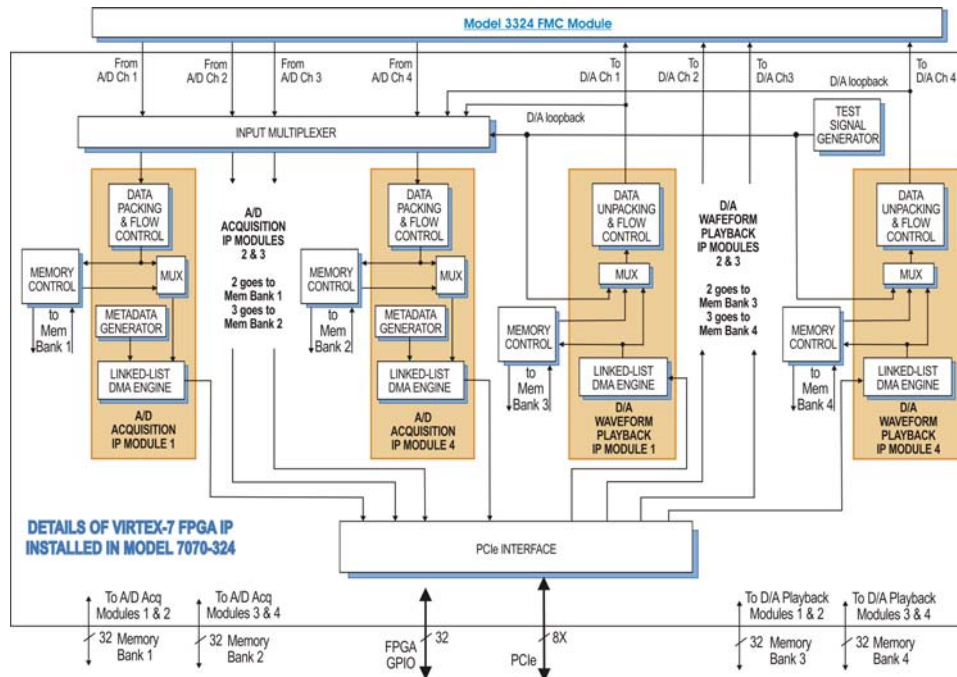
The board-set features four A/D Acquisition IP Modules for easily capturing and moving data. Each module can receive data from any of the four A/Ds, a test signal generator or from the D/A waveform playback IP module in loopback mode.

When used with a Pentek FMC carrier, the 3324 features four sophisticated D/A waveform playback IP modules. A linked-list controller allows users to easily play back via the D/As waveforms stored in either on-board or off-board host memory.

Products

4-Channel 500 MHz 16-bit A/D, 4-Channel 2 GHz 16-bit D/A - x8 PCIe

x8 PCIe FlexorSet 7070-324 or 3U VPX FlexorSet 5973-324



GateFlow
 ReadyFlow
 OnyxFx
 Gatepress
 See page 27

Figure 82

Models [7070-324](#) and [5973-324](#) are members of the FlexorSet family of high-performance x8 PCIe or 3U VPX boards based on the Xilinx Virtex-7 FPGA.

As a FlexorSet integrated solution, the Model 3324 FMC is factory-installed on the 7070 or 5973 carrier. The required FPGA IP is installed and the board-set is delivered ready for immediate use.

The delivered FlexorSet is a multichannel, high-speed data converter and is suitable for connection to the HF or IF ports of a communications or radar system. Its built-in data capture and playback features offer an ideal turnkey solution as well as a platform for developing and deploying custom FPGA-processing IP.

Each FlexorSet includes four 500 MHz, 16-bit A/Ds, four digital upconverters, four 2 GHz, 16-bit D/As, and four banks of memory. In addition to supporting PCIe Gen. 3 as a native interface, these models include optional copper and optical connections to the Virtex-7 FPGA for custom I/O.

When delivered as an assembled board-set, these models include factory-installed applications ideally matched to the board's analog interfaces. The functions include four A/D acquisition IP modules for simplifying data capture and data transfer. Each of the four acquisition IP modules contains IP modules for DDR3 SDRAM memories.

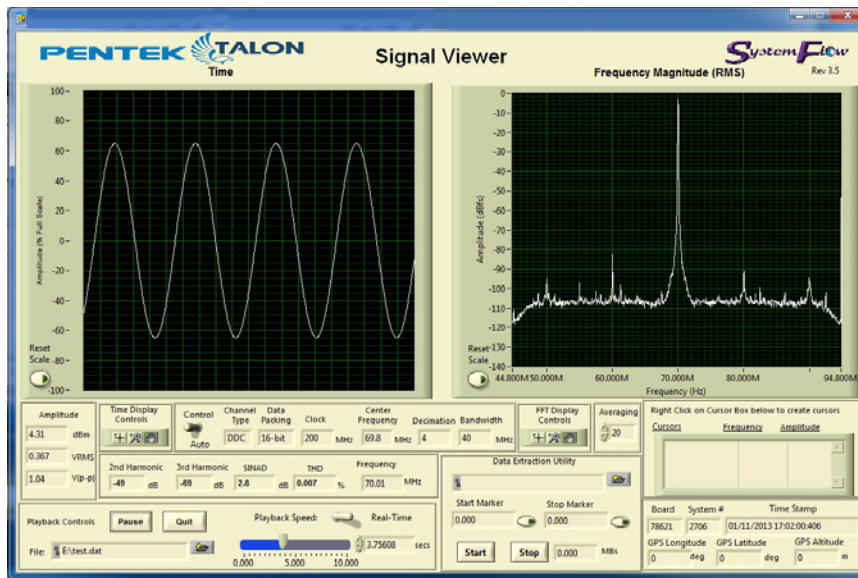
Each FlexorSet features four sophisticated D/A waveform playback IP modules. A linked-list controller allows users to easily play back to the D/As waveforms stored in either on-board or off-board host memory. Parameters including length of waveform, delay from playback trigger, waveform repetition, etc. can be programmed for each waveform. In each playback module, up to 64 individual link entries can be chained together to create complex waveforms with a minimum of programming.

A controller for all data clocking and synchronization functions, a test signal generator and a PCIe interface complete the factory-installed functions and enable these models to operate as turnkey solutions without the need to develop any FPGA IP.

Products

PC Development System for PCIe Cobalt, Onyx, Jade and Flexor Boards

Model 8266



Model 8266

SPARK
Development Systems

ReadyFlow
Board Support Package

Figure 83

The Model [8266](#) is a fully-integrated PC development system for Pentek Cobalt, Onyx, Jade and Flexor PCI Express software radio, data acquisition, and I/O boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

A fully-integrated system-level solution, the 8266 provides the user with a streamlined out-of-the-box experience. It comes preconfigured with Pentek hardware, drivers and software examples installed and tested to allow development engineers to run example applications out of the box.

Pentek ReadyFlow drivers and board support libraries are preinstalled and tested with the 8266. ReadyFlow includes example applications with full source code, a command line interface for custom

control over hardware, and Pentek's Signal Analyzer, a full-featured analysis tool that continuously displays live signals in both time and frequency domains.

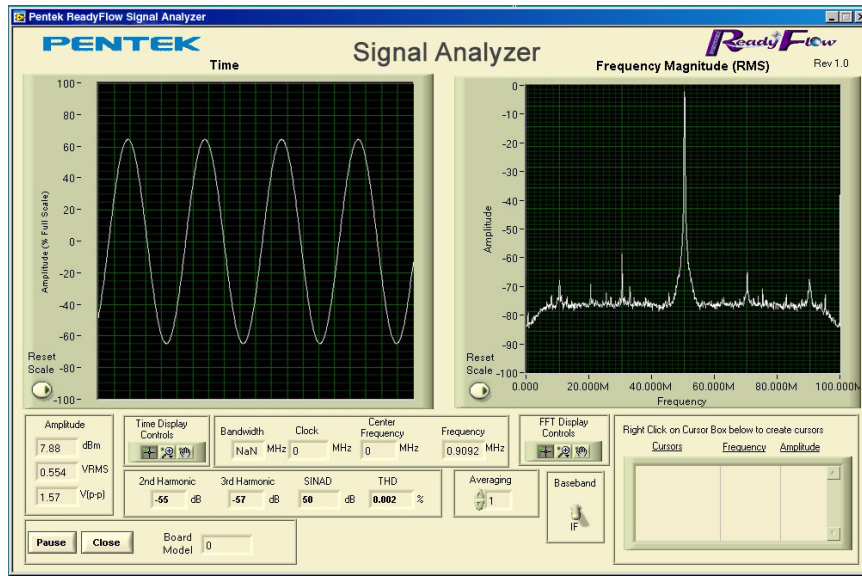
Built on a professional 4U rackmount workstation, the 8266 is equipped with the latest Intel processor, DDR3 SDRAM and a high-performance motherboard. These features accelerate application code development and provide unhindered access to the high-bandwidth data available with Cobalt, Onyx, Jade and Flexor analog and digital interfaces. The 8266 can be configured with 64-bit Windows or Linux operating systems.

The [8266](#) uses a 19" 4U rackmount chassis that is 21" deep. Enhanced forced-air ventilation assures adequate cooling for Pentek boards. A 1000-W power supply guarantees more than enough power for additional boards.

Products

3U OpenVPX Development System for Cobalt, Onyx, Jade and Flexor Boards

Model 8267



[Model 8267](#)

SPARK
Development Systems

ReadyFlow
Board Support Package

Figure 84

The Model [8267](#) is a fully-integrated, 3U OpenVPX development system for Pentek Cobalt, Onyx, Jade and Flexor software radio, data acquisition, and I/O boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

A fully-integrated system-level solution, the 8267 provides the user with a streamlined out-of-the-box experience. It comes preconfigured with Pentek hardware, drivers and software examples installed and tested to allow development engineers to run example applications out of the box.

Pentek ReadyFlow drivers and board support libraries are preinstalled and tested with the 8267. ReadyFlow includes example applications with full source code, a command line interface for custom control over

hardware, and Pentek's Signal Analyzer, a full-featured analysis tool that continuously displays live signals in both time and frequency domains.

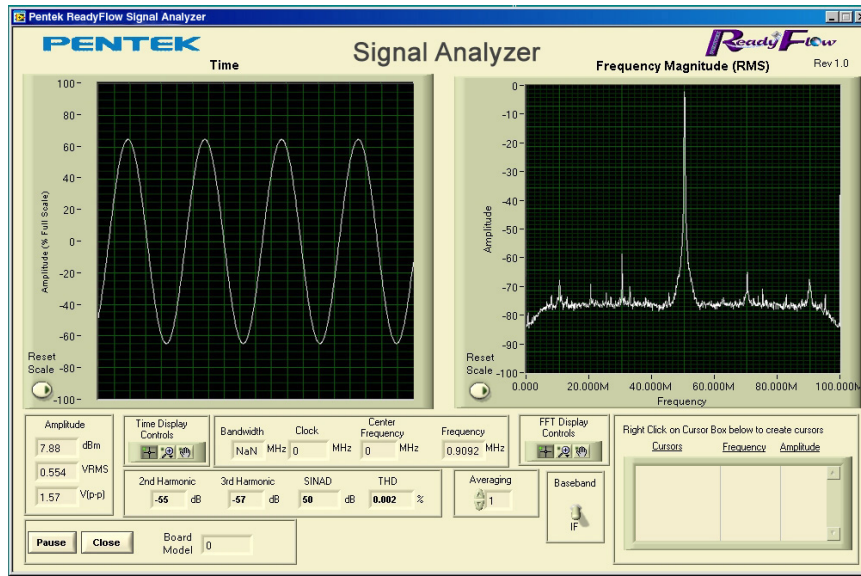
Built on a professional 4U rackmount workstation, the 8267 is equipped with the latest Intel i7 processor, DDR3 SDRAM and a high-performance single-board computer. These features accelerate application code development and provide unhindered access to the high-bandwidth data available with Cobalt, Onyx, Jade and Flexor analog and digital interfaces. The 8267 can be configured with 64-bit Windows or Linux operating systems.

The [8267](#) uses a 19" 4U rackmount chassis that is 12" deep. Nine VPX slots provide ample space for an SBC, a switch card and multiple Pentek boards. Enhanced forced-air ventilation assures adequate cooling for all boards and dual 250-W power supplies guarantee more than adequate power for all installed boards.

Products

6U OpenVPX Development System for Cobalt, Onyx and Jade Boards

Model 8264



SPARK
Development Systems

ReadyFlow
Board Support Package

Figure 85

The Model [8264](#) is a fully-integrated, 6U OpenVPX development system for Pentek Cobalt, Onyx and Jade software radio, data acquisition, and I/O boards. It was created to save engineers and system integrators the time and expense associated with building and testing a development system that ensures optimum performance of Pentek boards.

A fully-integrated system-level solution, the 8264 provides the user with a streamlined out-of-the-box experience. It comes preconfigured with Pentek hardware, drivers and software examples installed and tested to allow development engineers to run example applications out of the box.

Pentek ReadyFlow drivers and board support libraries are preinstalled and tested with the 8264. ReadyFlow includes example applications with full source code, a command line interface for custom control over

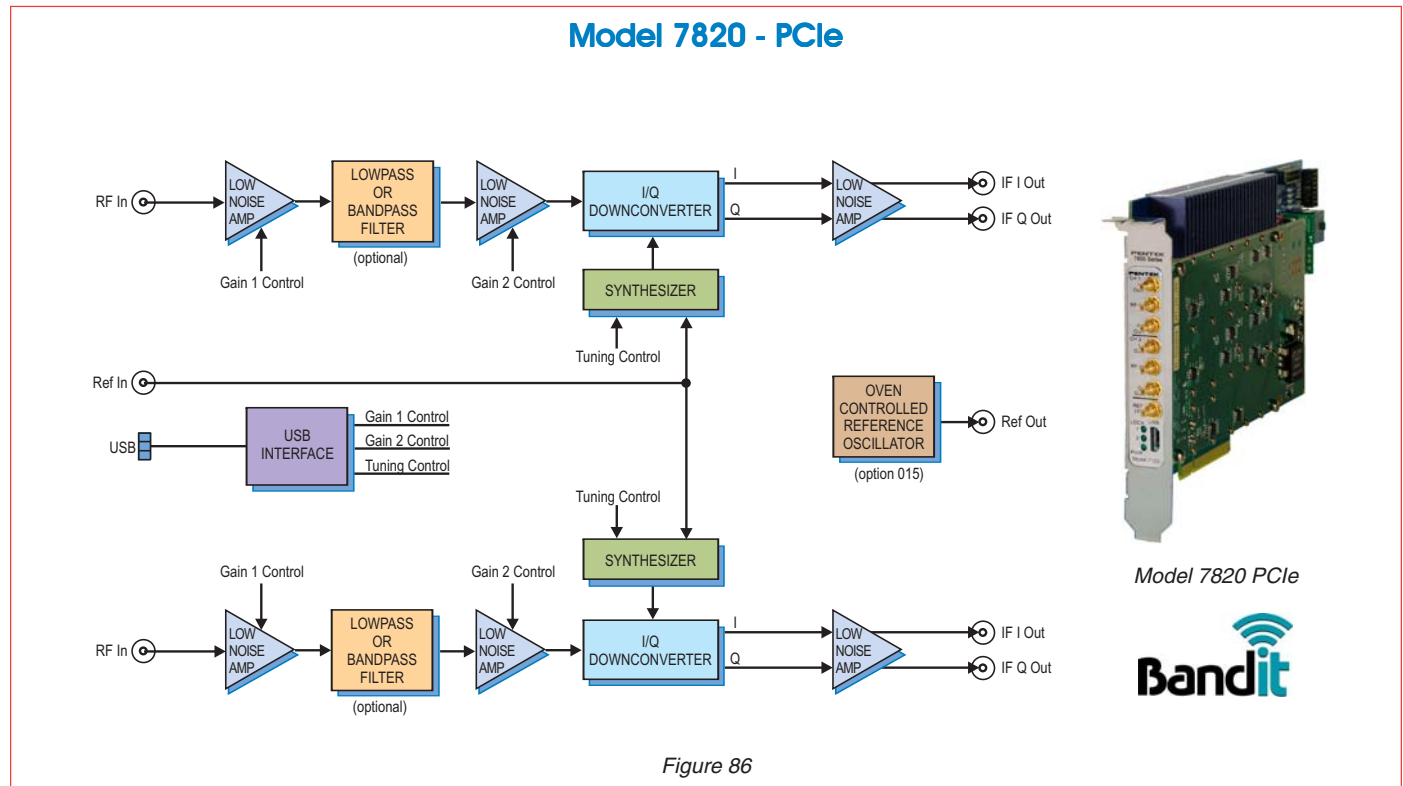
hardware, and Pentek's Signal Analyzer, a full-featured analysis tool that continuously displays live signals in both time and frequency domains.

Built on a professional 6U rackmount workstation, the 8264 is equipped with the latest Intel i7 processor, DDR3 SDRAM and a high-performance single-board computer. These features accelerate application code development and provide unhindered access to the high-bandwidth data available with Cobalt, Onyx and Jade analog and digital interfaces. The 8264 can be configured with 64-bit Windows or Linux operating systems.

The [8264](#) uses a 19" 6U rackmount chassis that is 12" deep. Nine VPX slots provide ample space for an SBC, a switch card and multiple Pentek boards. Enhanced forced-air ventilation assures adequate cooling for all boards and dual 500-W power supplies guarantee more than adequate power for all installed boards.

Complementary Products

Bandit Two-Channel Analog RF Wideband Downconverter



The Bandit® Model 7820 is a two-channel, high-performance, stand-alone analog RF wideband down-converter. Packaged in a small, shielded PCIe board with front-panel connectors for easy integration into RF systems, the board offers programmable gain, high dynamic range and a low noise figure.

With an input frequency range from 400 to 4000 MHz and a wide IF bandwidth of up to 390 MHz, the 7820 is an ideal solution for amplifying and downconverting antenna signals for communications, radar and SIGINT.

The 7820 accepts RF signals on two front-panel SSMC connectors. LNAs (Low Noise Amplifiers) are provided, along with two programmable attenuators allowing downconversion of input signals ranging from -60 dBm to -20 dBm in steps of 0.5 dB. Higher level signals can be attenuated prior to input. An optional five-stage lowpass or bandpass input filter can be included with several available frequency and attenuation characteristics for RF image rejection and harmonic

suppression. The 7820 features a pair of Analog Devices ADL5380 quadrature mixers. The ADL5380's are capable of excellent accuracy with amplitude and phase balances of ~ 0.07 dB and $\sim 0.2^\circ$, respectively.

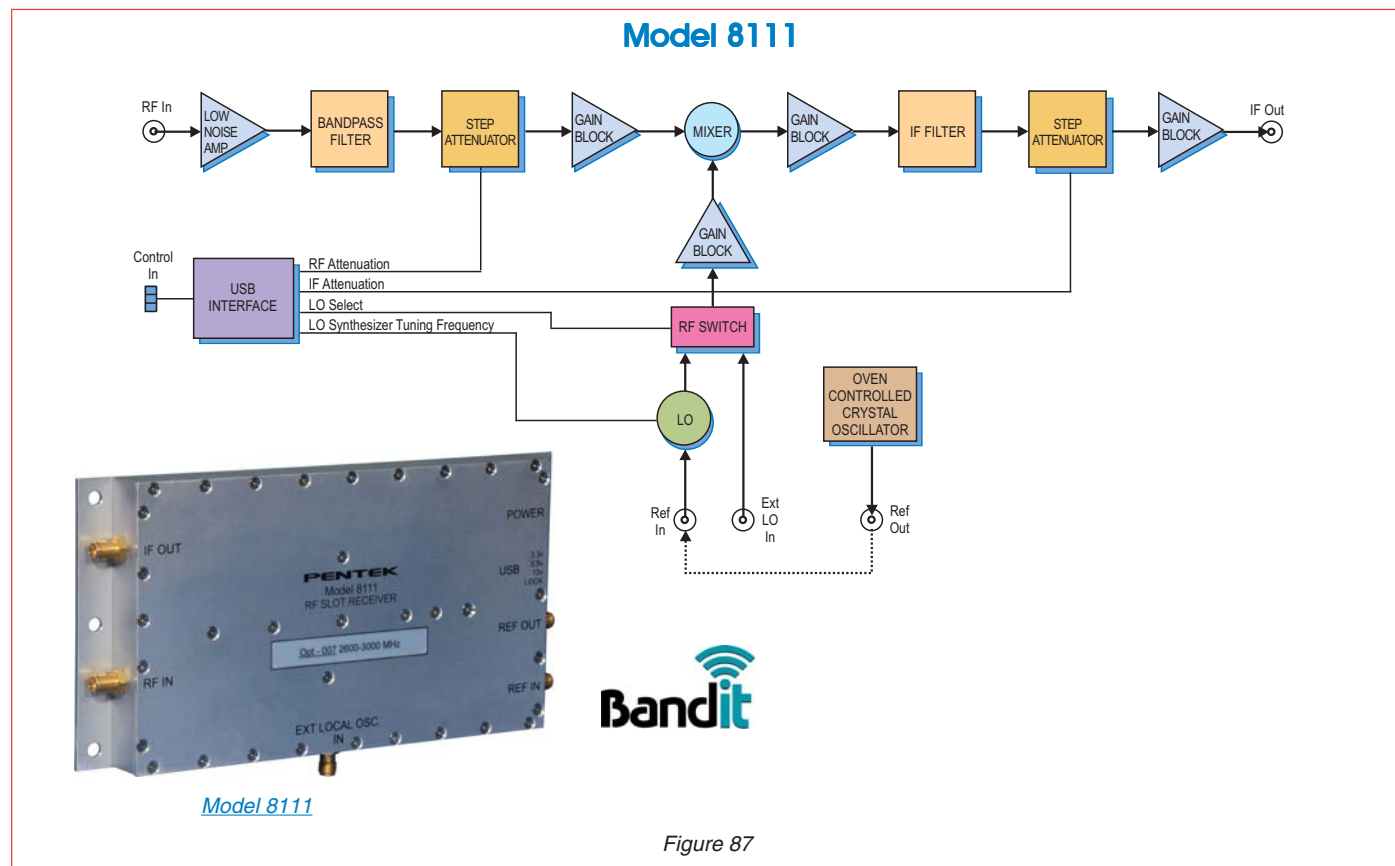
The 7820 uses an Analog Devices ADF4351 low-noise, on-board frequency synthesizer as the LO (Local Oscillator). Locked to an external input reference for accuracy with a fractional-N phase-locked loop, its frequency is programmable across the 400 to the 4000 MHz band with a tuning resolution of better than 100 kHz.

Output is provided as baseband I and Q signals at bandwidths up to 390 MHz. User-provided in-line output IF filters allow customizing the output bandwidth and offset frequency to the specific application requirements.

Versions of the [7820](#) are also available as an XMC module (Model [7120](#)), 3U VPX (Models [5220](#) and [5320](#)), 6U VPX (Models [5720](#) and [5820](#) with dual density), AMC (Model [5620](#)), 6U cPCI (Models [7220](#) and [7420](#) with dual density), and 3U cPCI (Model [7320](#)).

Complementary Products

Bandit Modular Analog RF Downconverter Series



The Bandit Model [8111](#) provides a series of high-performance, stand-alone RF slot receiver modules. Packaged in a small, shielded enclosure with connectors for easy integration into RF systems, the modules offer programmable gain, high dynamic range and a low noise figure. With input options to cover specific frequency bands of the RF spectrum, and an IF output optimized for A/D converters, the 8111 is an ideal solution for amplifying and downconverting antenna signals for communications, radar and signal intelligence systems.

The 8111 accepts RF signals on a front panel SMA connector. An LNA (Low Noise-figure Amplifier) is provided along with two programmable attenuators allowing downconversion of input signals ranging from -60 dBm to -20 dBm in steps of 0.5 dB. Higher level signals can be attenuated prior to input.

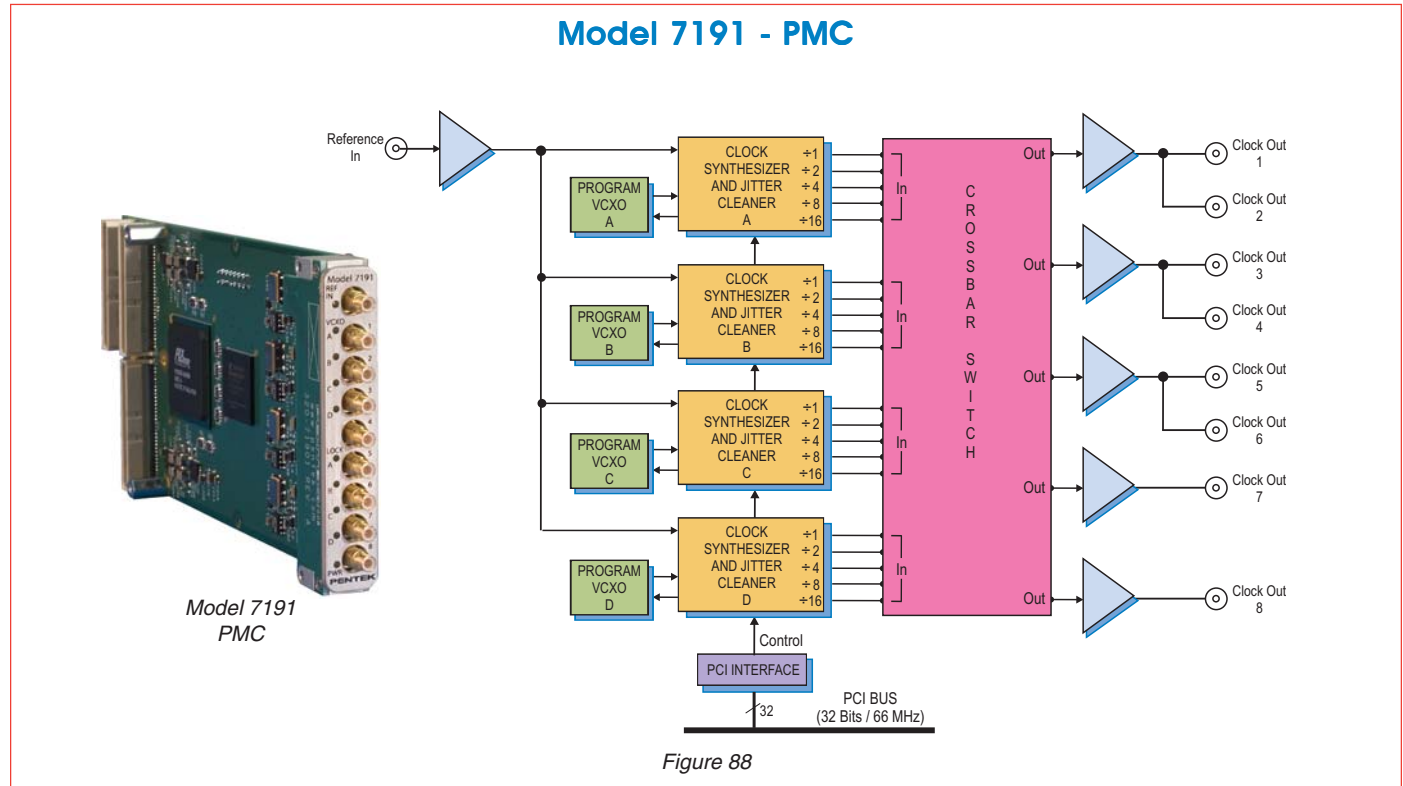
Seven different input-frequency band options are offered, each tunable across a 400 MHz band, with an overlap of 100 MHz between adjacent bands. As a group, these seven options accommodate RF input signals from 800 MHz to 3.000 GHz as follows:

Option	Frequency Band
001	800-1200 MHz
002	1100-1500 MHz
003	1400-1800 MHz
004	1700-2100 MHz
005	2000-2400 MHz
006	2300-2700 MHz
007	2600-3000 MHz

An 80 MHz-wide IF output is provided at a 225 MHz center frequency. This output is suitable for A/D conversion using Pentek high-performance signal acquisition products, such as those in the Cobalt, Onyx or Jade families.

Complementary Products

Programmable Multifrequency Clock Synthesizer



Model 7191 generates up to eight synthesized clock signals suitable for driving A/D and D/A converters in high-performance real-time data acquisition and software radio systems. The clocks offer exceptionally low phase noise and jitter to preserve the signal quality of the data converters. These clocks are synthesized from programmable VCXOs and can be phase-locked to an external reference signal.

The 7191 uses four Texas Instruments CDC7005 clock synthesizer and jitter cleaner devices. Each CDC7005 is paired with a dedicated VCXO to provide the base frequency for the clock synthesizer. Each of the four VCXOs can be independently programmed to a desired frequency between 50 MHz and 700 MHz with 32-bit tuning resolution.

The CDC7005 can output the programmed frequency of its associated VCXO, or generate submultiples using divisors of 2, 4, 8 or 16. The four CDC7005's can output up to five frequencies each. The 7191 can be programmed to route any of these 20 frequencies to the module's five output drivers.

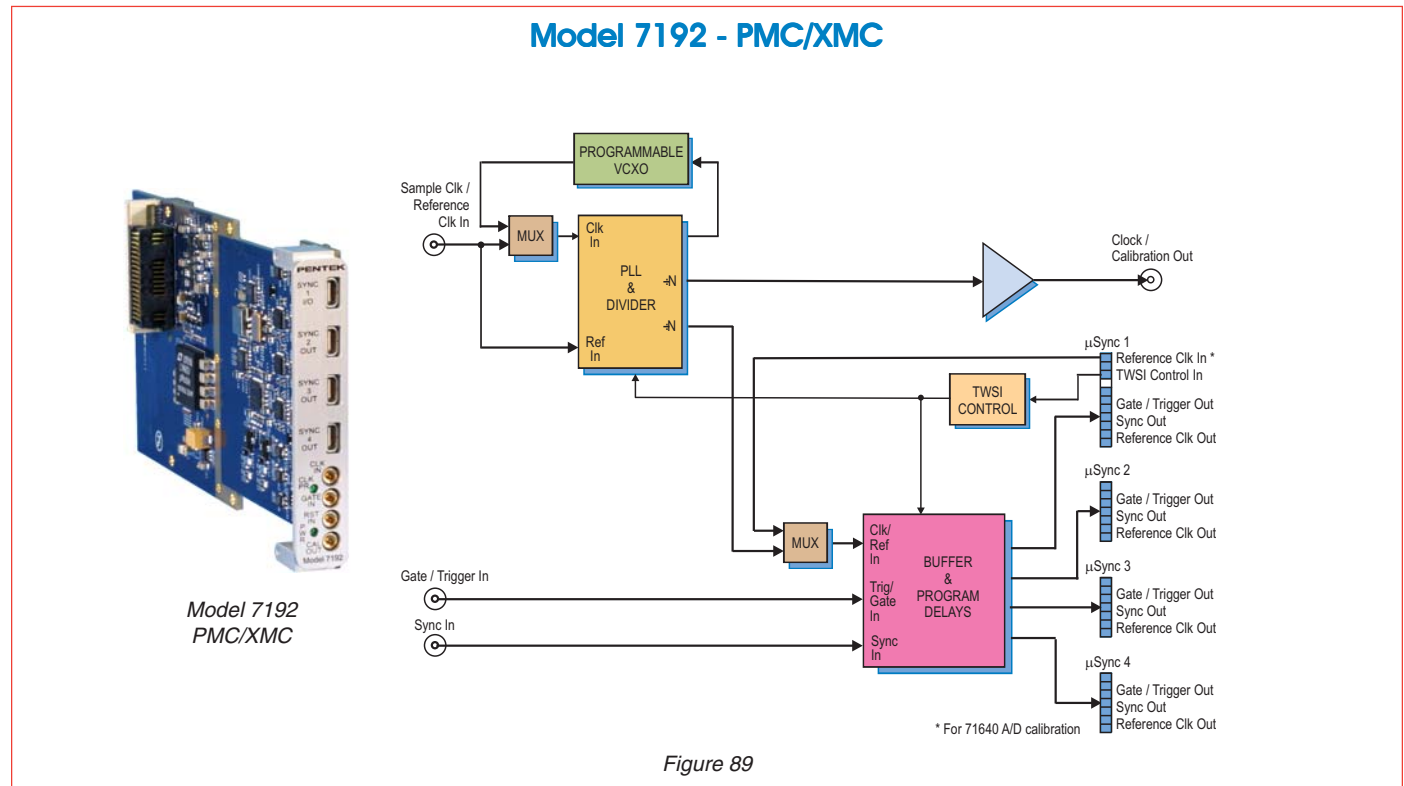
The CDC7005 includes phase-locking circuitry that locks the frequency of its associated VCXO to an input reference of 5 MHz to 100 MHz.

Eight front panel SMC connectors supply synthesized clock outputs driven from the five clock output drivers. This supports a single identical clock to all eight outputs or up to five different clocks to various outputs. With four programmable VCXOs and each CDC7005 capable of providing up to five different submultiple clocks, a wide range of clock configurations is possible. In systems where more than five different clock outputs are required simultaneously, multiple 7191's can be used and phase-locked with the 5 MHz to 100 MHz system reference.

Versions of the [7191](#) are also available as a PCIe half-length board (Model [7891](#)), 3U VPX board (Model [5391](#)), 6U VPX (Models [5791](#) and [5891](#) with dual density), AMC (Model [5691](#)), PCI board (Model [7691](#)), 6U cPCI (Models [7291](#) and [7291D](#) dual density), or 3U cPCI (Model [7391](#)).

Complementary Products

High-Speed Synchronizer and Distribution Board



The Model 7192 High-Speed Synchronizer and Distribution Board synchronizes multiple Pentek Cobalt or Onyx modules within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP, and software radio applications. Up to four modules can be synchronized using the 7192, with each receiving a common clock along with timing signals that can be used for synchronizing, triggering and gating functions.

Model 7192 provides three front panel MMCX connectors to accept input signals from external sources: one for clock, one for gate or trigger and one for a synchronization signal. Clock signals can be applied from an external source such as a high performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. In addition to the MMCX connector, a reference clock can be accepted through the first front panel μ Sync output connector, allowing a single Cobalt or Onyx board to generate the clock for all subsequent boards in the system.

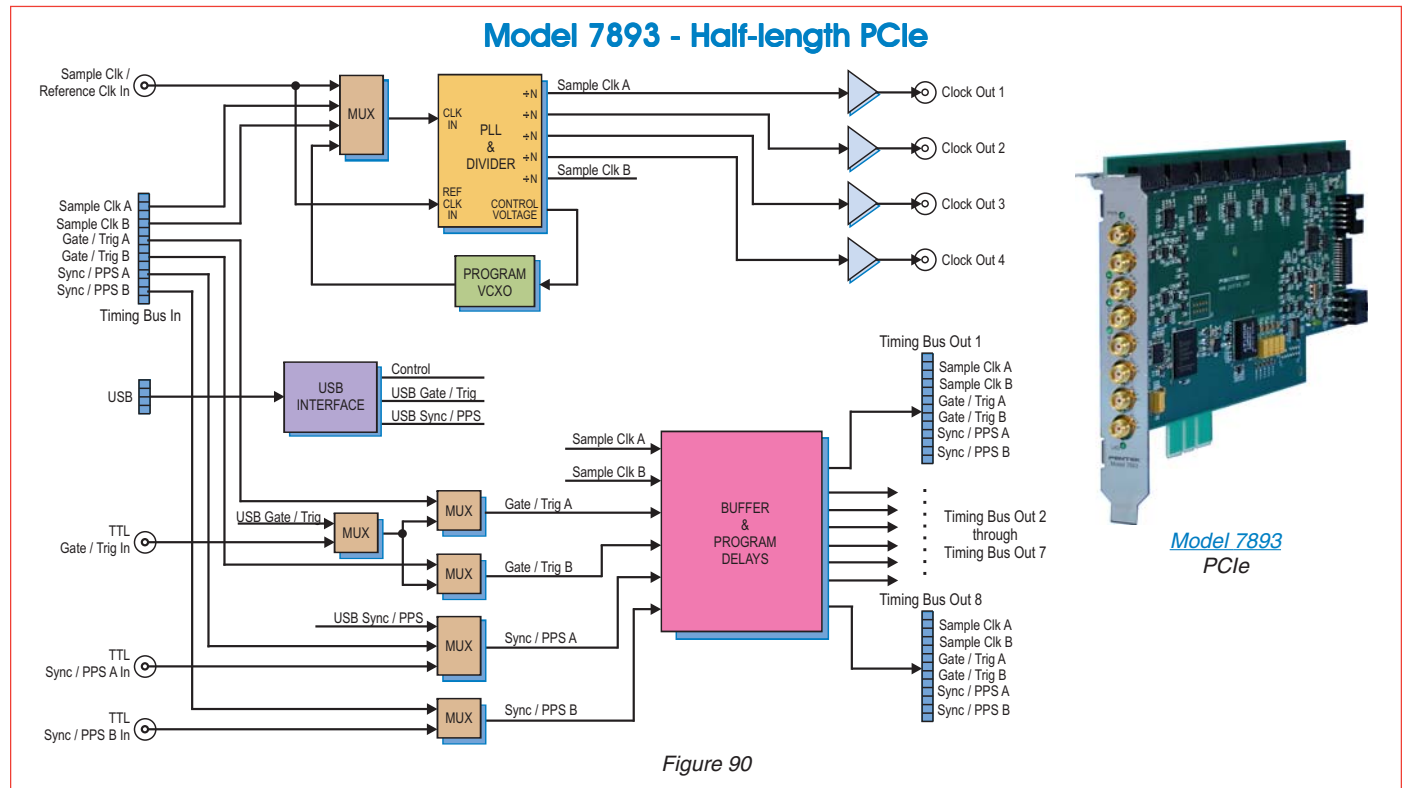
The 7192 provides four front panel μ Sync output connectors, compatible with a range of high-speed Pentek Cobalt and Onyx modules. The μ Sync signals include a reference clock, gate/trigger and sync signals and are distributed through matched cables, simplifying system design. The 7192 features a calibration output specifically designed to work with the 71640 or 71740 3.6 GHz A/D module and provide a signal reference for phase adjustment across multiple D/As.

The 7192 supports all high-speed models in the Cobalt and Onyx families including the 71630/71730 1 GHz A/D and D/A XMC, the 71640/71741 3.6 GHz A/D XMC and the 71670/71771 Four-channel 1.25 GHz, 16-bit D/A XMC.

Versions of the 7192 are also available as a PCIe half-length board (Model 7892), 3U VPX (Model 5292), 6U VPX (Models 5792 and 5892 with dual density), AMC (Model 5692), 6U cPCI (Models 7292 and 7492 dual density), and 3U cPCI (Model 7392).

Complementary Products

System Synchronizer and Distribution Board



Model [7893](#) System Synchronizer and Distribution Board synchronizes multiple Pentek Cobalt, Onyx and Jade boards within a system. It enables synchronous sampling, playback and timing for a wide range of multichannel high-speed data acquisition, DSP and software radio applications.

Up to eight boards can be synchronized using the 7893, each receiving a common clock up to 800 MHz along with timing signals that can be used for synchronizing, triggering and gating functions. For larger systems, up to eight 7893s can be linked together to provide synchronization for up to 64 Cobalt or Onyx boards.

The Model 7893 provides four front panel SMA connectors to accept LVTTTL input signals from external sources: two for Sync/PPS and one for Gate/Trigger. In addition to the synchronization signals, a front panel SMA connector accepts sample clocks up to 800 MHz or, in an alternate mode, accepts a 10 MHz reference clock to lock an on-board VCXO sample clock source.

The 7893 provides eight timing bus output connectors for distributing all needed timing and clock signals to the front panels of Cobalt, Onyx and Jade boards via ribbon cables. The 7893 locks the Gate/Trigger and Sync/PPS signals to the system's sample clock. The 7893 also provides four front panel SMA connectors for distributing sample clocks to other boards in the system.

The 7893 can accept a clock from either the front panel SMA connector or from the timing bus input connector. A programmable on-board VCXO clock generator can be locked to a user-supplied, 10 MHz reference.

The [7893](#) supports a wide range of products in the Cobalt family including the 78620 and 78621 three-channel A/D 200 MHz transceivers, the 78650 and 78651 two-channel A/D 500 MHz transceivers, the 78660, 78661 and 78662 four-channel 200 MHz A/Ds, and the 78690 L-Band RF Tuner. The 7893 also supports the Onyx 78760 four-channel 200 MHz A/D and all complementary models in the Onyx and Jade families.

Complementary Products

High-Speed Clock Generator

Model 7194 - PMC/XMC

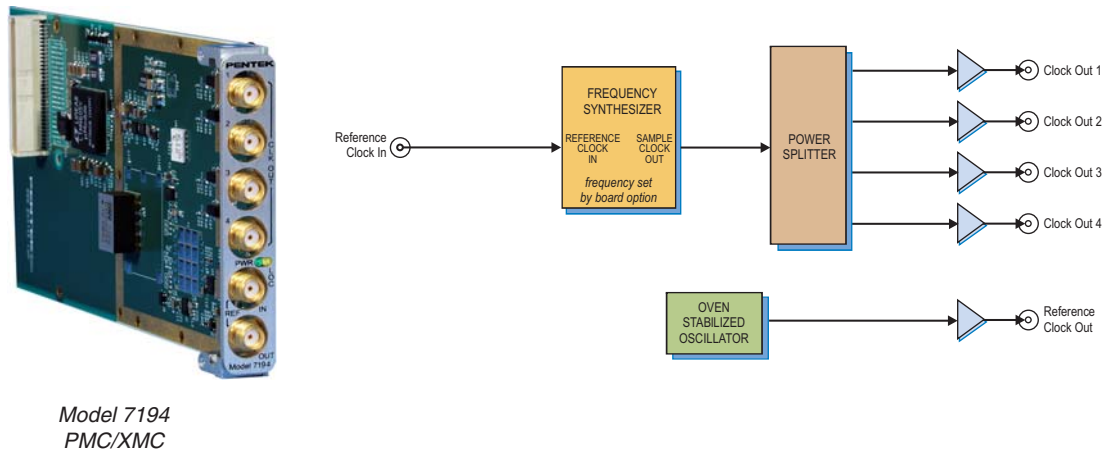


Figure 91

Model 7194 High-Speed Clock Generator provides fixed-frequency sample clocks to Cobalt, Onyx, Jade and Flexor modules in multiboard systems. It enables synchronous sampling, playback and timing for a wide range of multichannel high-speed data acquisition and software radio applications.

The Model 7194 uses a high-precision, fixed-frequency, PLO (Phase-Locked Oscillator) to generate an output sample clock. The PLO accepts a 10 MHz reference clock through a front panel SMA connector. The PLO locks the output sample clock to the incoming reference. A power splitter then receives the sample clock and distributes it to four front panel SMA connectors.

The 7194 is available with sample clock frequencies from 1.4 to 2.0 GHz.

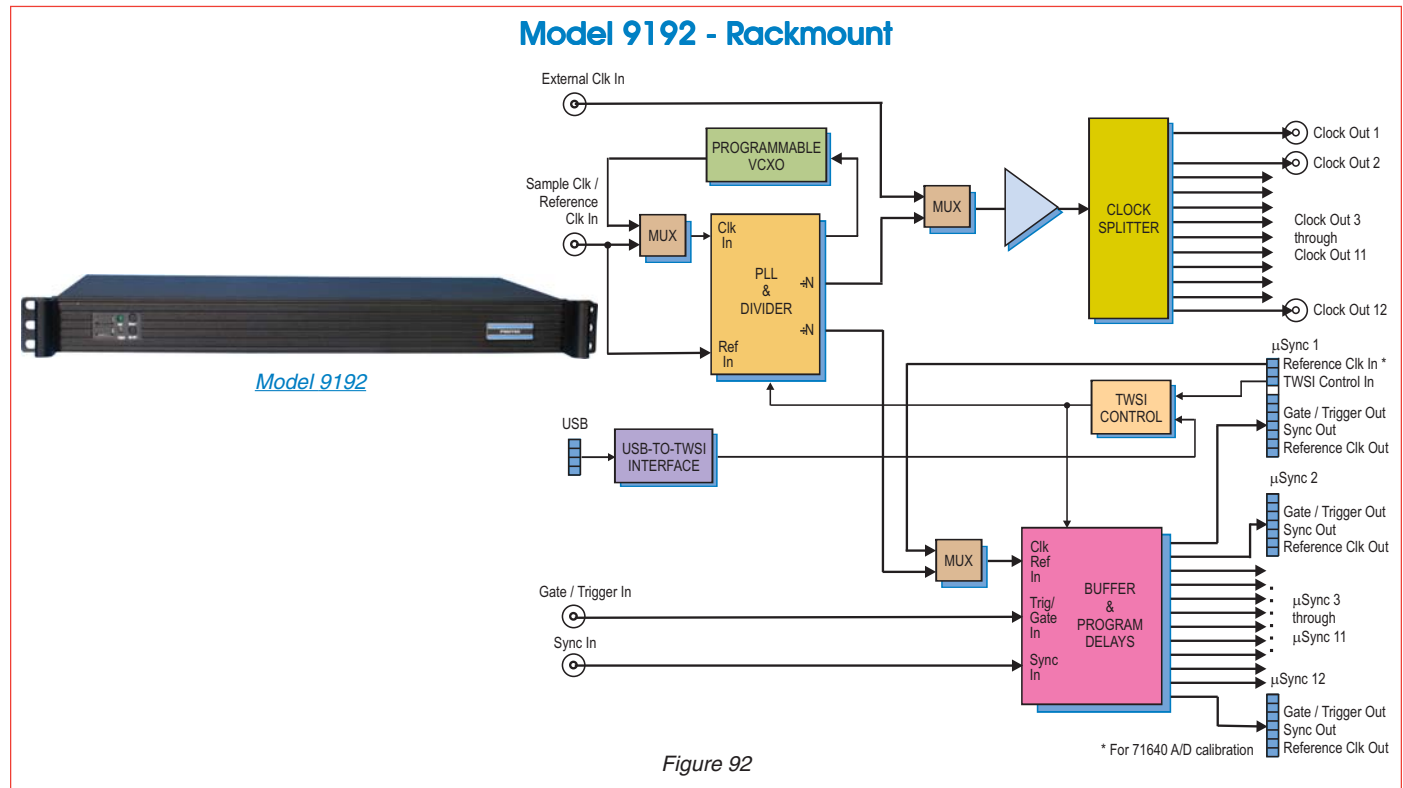
In addition to accepting a reference clock on the front panel, the 7194 includes an on-board 10 MHz reference clock. The reference is an OCXO (Oven-Controlled Crystal Oscillator), which provides an exceptionally precise frequency standard with excellent phase noise characteristics.

The 7194 is a standard PMC/XMC module. The module does not require programming and the PMC P14 or XMC P15 connector is used solely for power. The module can be optionally configured with a PCIe-style 6-pin power connector allowing it to be used in virtually any chassis or enclosure.

Versions of the [7194](#) are also available as a PCIe half-length board (Model [7894](#)), 3U VPX (Model [5294](#)), 6U VPX (Models [5794](#) and [5894](#) with dual density), AMC (Model [5694](#)), 6U cPCI (Models [7294](#) and [7494](#) dual density), and 3U cPCI (Model [7394](#)).

Complementary Products

High-Speed System Synchronizer Unit



Model [9192](#) Rack-mount High-Speed System Synchronizer Unit synchronizes multiple Pentek Cobalt, Onyx, Jade or Flexor boards within a system. It enables synchronous sampling and timing for a wide range of multichannel high-speed data acquisition, DSP, and software radio applications. Up to twelve boards can be synchronized using the 9192, each receiving a common clock along with timing signals that can be used for synchronizing, triggering and gating functions.

Model 9192 provides four rear panel SMA connectors to accept input signals from external sources: two for clock, one for gate or trigger and one for a synchronization signal. Clock signals can be applied from an external source such as a high performance sine-wave generator. Gate/trigger and sync signals can come from an external system source. In addition to the SMA connector, a reference clock can be accepted through the first rear panel μ Sync output connector, allowing a single Cobalt or Onyx board to generate the clock for all subsequent boards in the system.

The 9192 provides four rear panel μ Sync output connectors, compatible with a range of high-speed Pentek boards. The μ Sync signals include a reference clock, gate/trigger and sync signals and are distributed through matched cables, simplifying system design.

The 9192 features twelve calibration outputs specifically designed to work with the 71640 or 71741 3.6 GHz A/D modules and provides a signal reference for phase adjustment across multiple D/As.

The 9192 allows programming of operation parameters including: VCXO frequency, clock dividers, and delays that allow the user to make timing adjustments on the gate and sync signals. These adjustments are made before they are sent to buffers for output through the μ Sync connectors.

The [9192](#) supports all high-speed models in the Cobalt family including the 71630 1 GHz A/D and D/A XMC, the 71640 3.6 GHz A/D XMC and the 71670 Four-channel 1.25 GHz, 16-bit D/A XMC. The 9192 also supports high-speed models in the Onyx and Jade families.

Complementary Products

Talon High-Speed Recording Systems: Flexible and Deployable Solutions

High-Speed Recording Systems

Talon® High-Speed Recording Systems eliminate the time and risk associated with new technology system development. With increasing pressure in both the defense and commercial arenas to get to the market first, today's system engineers are looking for more complete off-the-shelf system offerings.

Out of the box, these systems arrive complete with a full-featured virtual operator control panel ready for immediate data recording and/or playback operation.

Because they consist of modular COTS board-level products and the flexible Pentek SystemFlow® software, they are easily scalable to larger multichannel data acquisition and recording applications requiring aggregate recording rates of up to 5.0 GB/sec.

Ready-to-Run Recording Systems

Depending on model, the Pentek offerings are fully integrated systems featuring a range of A/D and D/A resources or digital I/O with high-speed disk arrays.

These systems are built on a Windows workstation and they are presented in this section because they can easily satisfy a broad spectrum of recording needs. Furthermore, users can easily install postprocessing and analysis tools to operate on the recorded data which is stored in the familiar NTFS format.



RTV Recording Systems are excellent value for under \$20,000 US



RTS Recording Systems are designed for commercial applications



RTR Recording Systems are designed for harsh environments



RTX Recording Systems are designed for extreme environments

ANALOG RECORDERS

[Click Here for the SYSTEM SELECTOR](#)

DIGITAL RECORDERS

[Click Here for the SYSTEM SELECTOR](#)

Recording Systems Form Factors

Pentek's High-Speed Recording Systems are available as Lab Systems, Portable Systems, Rugged, and Extreme Systems.

RTV and RTS Lab Systems are housed in a 19-in. rack-mountable chassis in a PC server configuration. They are designed for commercial applications in a lab or office environment.



RTS Lab system

RTR Portable Systems are available in a small briefcase-sized enclosures with integral LCD display and keyboard. They, too, provide a PC server configuration and are designed for harsh environment field applications where size and weight is of paramount importance.



RTR Portable System

RTR Rugged Rackmount Systems are housed in a 19-in. rugged rack-mountable chassis. They are built to survive shock and vibration and they target operation in harsh environments and remote locations that may be unsuitable for humans.



RTR Rackmount system

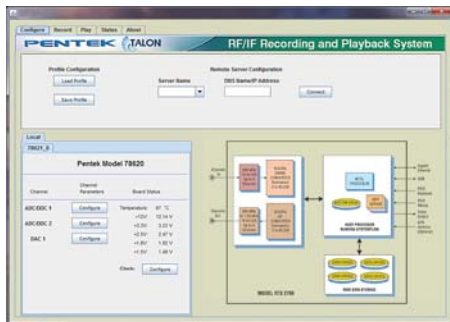
RTX Extreme Systems are available in a rackmount chassis designed to military specs. They are designed to operate under extreme environmental conditions using forced-air or conduction-cooling to draw heat from system components.



RTX Rackmount system

Complementary Products

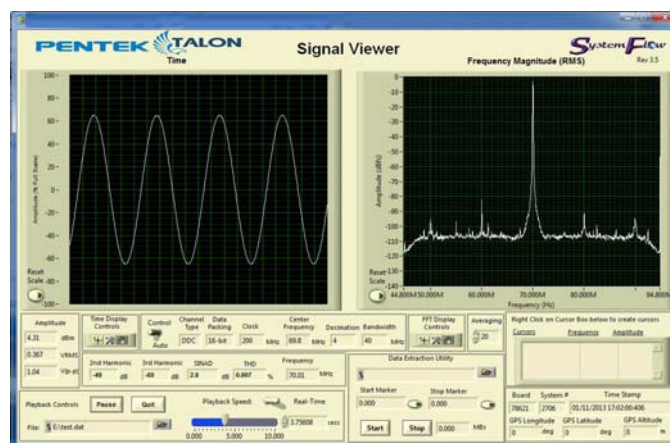
Pentek SystemFlow Recording Software for Analog Recorders



Recorder Interface



Hardware Configuration



Signal Viewer



Figure 93

The Pentek SystemFlow Recording Software for Analog Recorders provides a rich set of function libraries and tools for controlling all Pentek analog high-speed real-time recording systems. SystemFlow software allows developers to configure and customize system interfaces and behavior.

The **Recorder Interface** shows a system block diagram and includes configuration, record, playback and status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, play back a recorded signal and monitor board temperatures and voltage levels.

The **Hardware Configuration** screen provides a simple and intuitive means for setting up the system parameters. The configuration screen shown here, allows user entries for input source, center frequency, decimation, as well as gate and trigger information. All parameters

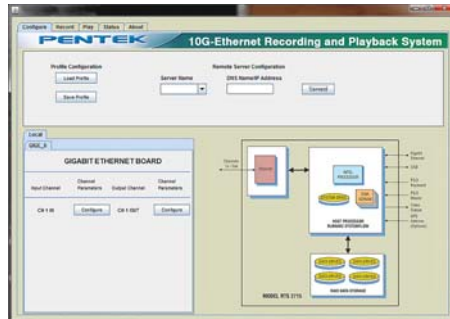
contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

The SystemFlow **Signal Viewer** includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded to help ensure successful recording sessions. The viewer can also be used to inspect and analyze the recorded files after the recording is complete.

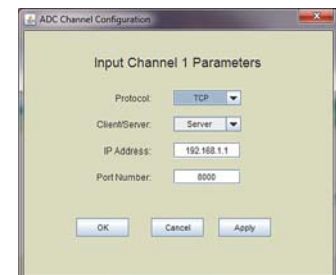
Advanced signal analysis capabilities include automatic calculators for signal amplitude and frequency, second and third harmonic components, THD (total harmonic distortion) and SINAD (signal to noise and distortion). With time and frequency zoom, panning modes and dual annotated cursors to mark and measure points of interest, the Signal Viewer can often eliminate the need for a separate oscilloscope or spectrum analyzer in the field.

Complementary Products

Pentek SystemFlow Recording Software for Digital Recorders



Main Interface



Hardware Configuration



Record Screen



Figure 94

The SystemFlow **Main Interface** for Digital Recorders shows a block diagram of the system and provides the user with a control interface for the recording system. It includes Configuration, Record, Playback, and Status screens, each with intuitive controls and indicators. The user can easily move between screens to set configuration parameters, control and monitor a recording, and play back a recorded stream.

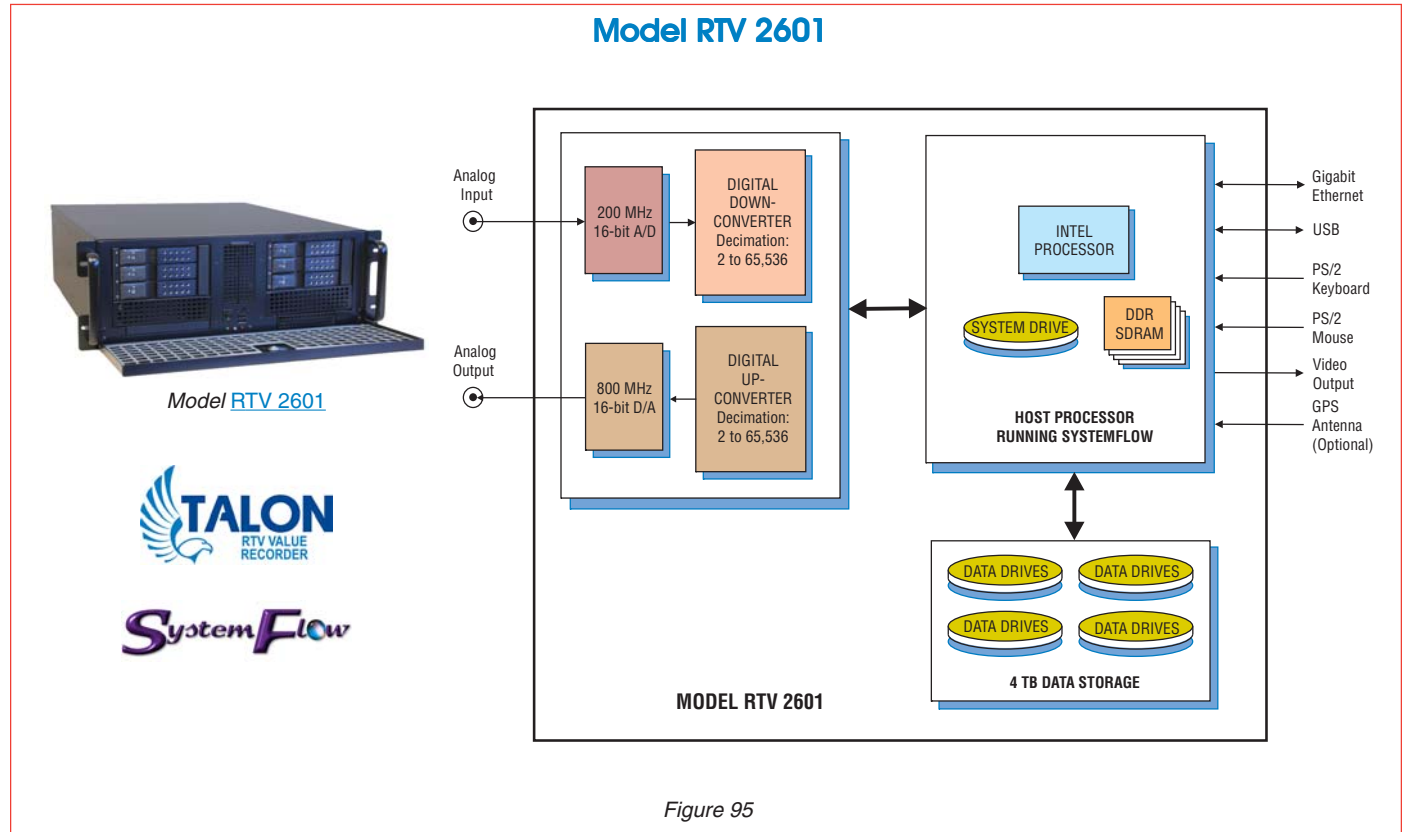
The **Configure** screen presents operational system parameters including temperature and voltages. Parameters are entered for each input or output channel specifying UDP or TCP protocol, client or server connection, the IP address and port number. All parameters contain limit-checking and integrated help to provide an easier-to-use out-of-the-box experience.

The **Record** screen allows you to browse a folder and enter a file name for the recording. The length of the recording for each channel can be specified in megabytes or in seconds. Intuitive buttons for Record, Pause and Stop simplify operation. Status indicators for each channel display the mode, the number of recorded bytes, and the average data rate. A Data Loss indicator alerts the user to any problem, such as a disk- full condition.

By checking the Master Record boxes, any combination of channels in the lower screen can be grouped for synchronous recording via the upper Master Record screen. The recording time can be specified, and monitoring functions inform the operator of recording progress.

Complementary Products

200 MS/sec RF/IF Rackmount Value Recorder



The Talon [RTV 2601](#) is a turnkey multiband recording and playback system used for recording and reproducing signals with bandwidths up to 80 MHz. The RTV 2601 uses a 16-bit, 200 MHz A/D converter to provide real-time sustained recording rates to disk of up to 400 MB/sec. The A/D is complemented with a 16-bit 800 MHz D/A that provides the ability to reproduce signals captured in the field.

The RTV 2601 comes in a 4U 19 in. rackmount package that is 22.75 in. deep. Signal I/O is provided in the rear of the unit, while the hot-swappable data drives are available at the front. Air is pulled through the system from front to back allowing it to operate at ambient temperatures from 5 to 35 deg C.

The RTV 2601 includes a programmable digital downconverter so users can configure the system to capture signals with frequencies as low as 300 kHz and as high as 700 MHz. Corresponding signal bandwidths range from

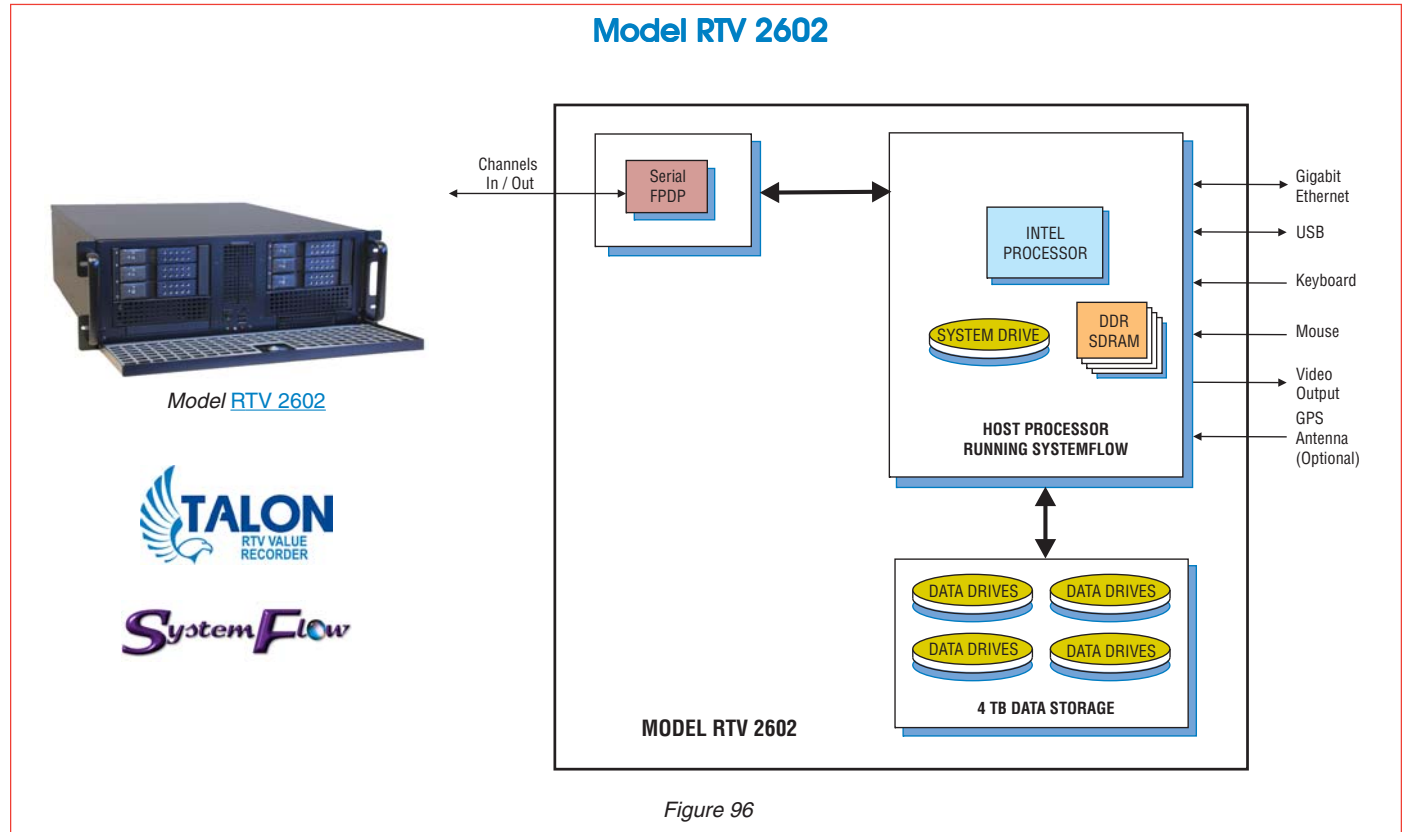
a few kilohertz to 80 MHz. A digital upconverter and D/A produce an analog output matching the recorded IF signal frequency.

The system includes a built-in sample clock synthesizer programmable to any desired frequency from 10 MHz to 200 MHz. This clock synthesizer can be locked to an external 10 MHz reference clock and has excellent phase noise characteristics. Alternately, the user can supply an external sample clock to drive the A/D and D/A converters. The RTV 2601 also supports external triggering, allowing users to trigger a recording or playback on an external signal.

The [RTV 2601](#) includes the Pentek SystemFlow recording software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the recorder. As an option, a GPS or IRIG receiver card can be supplied with the system for accurate time stamping of recorded data.

Complementary Products

Serial FPDP Rackmount Value Recorder



The Talon [RTV 2602](#) Serial FPDP Value Recorder is designed to provide a low-cost solution to users looking to capture and play back multiple Serial FPDP streams. It can record up to four Serial FPDP channels to the built-in 4 TB RAID consisting of cost-effective, enterprise-class HDD storage. It is a complete turnkey recording system, ideal for capturing any type of streaming sources. These include live transfers from sensors or data from other computers and is fully compatible with the VITA 17.1 specification.

The RTV 2602 comes in a 4U 19 in. rack-mount package that is 22.75 in. deep. Signal I/O is provided in the rear of the unit, while the hot-swappable data drives are available in the front. Air is pulled through the system from front to back to allow operation at ambient temperatures from 5° to 35° C.

The RTV 2606 can be populated with up to four SFP connectors supporting Serial FPDP over copper, single-

mode, or multi-mode fiber, to accommodate all popular Serial FPDP interfaces. It is capable of both receiving and transmitting data over these links and supports real-time data storage to disk.

Programmable modes include flow control in both receive and transmit directions, CRC support, and copy/loop modes. The system is capable of handling 1.0625, 2.125, 2.5, 3.125 and 4.25 GBaud link rates. Up to four channels can be recorded simultaneously with an aggregate recording rate of up to 400 MB/sec.

As an option, a GPS or IRIG receiver card can be supplied with the system providing accurate time stamping of recorded data. Additionally, the GPS receiver delivers GPS position information that can be recorded along with the input signals.

The [RTV 2602](#) includes the Pentek SystemFlow recording software which features a Windows-based GUI.

Complementary Products

200 MS/sec RF/IF Rugged Portable Recorder

Model RTR 2726A

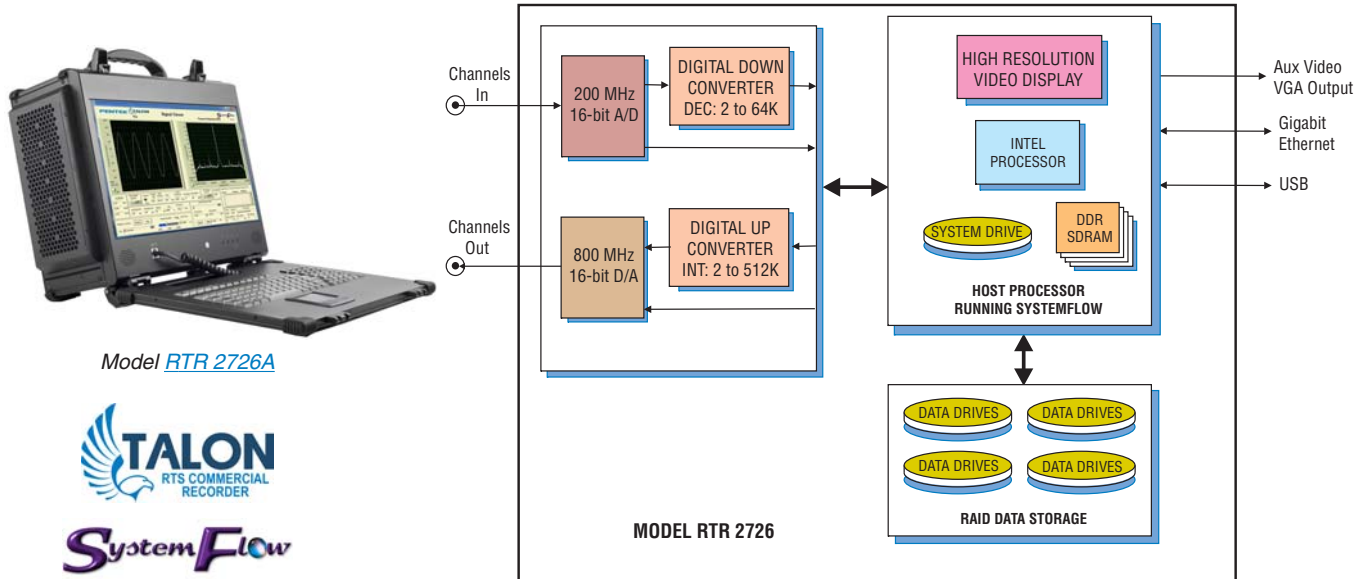


Figure 97

The Talon [RTR 2726A](#) is a turnkey, multiband recording and playback system that allows the user to record and reproduce high-bandwidth signals with lightweight, portable and rugged packages. This model provides aggregate recording rates of up to 3.2 GB/sec and is ideal for the user who requires both portability and solid performance in a compact recording system.

The RTR 2726A is supplied in a small footprint portable package measuring only 16.0" W x 6.9" D x 13.0" H and weighing just less than 30 pounds.

With measurements similar to small briefcases, this portable workstation includes Intel Core i7 processors, high-resolution 17" LCD monitors, and up to 15.3 TB of SSD storage.

A/D sampling rate, DDC decimation and bandwidth, D/A sampling rate and DUC interpolation are among

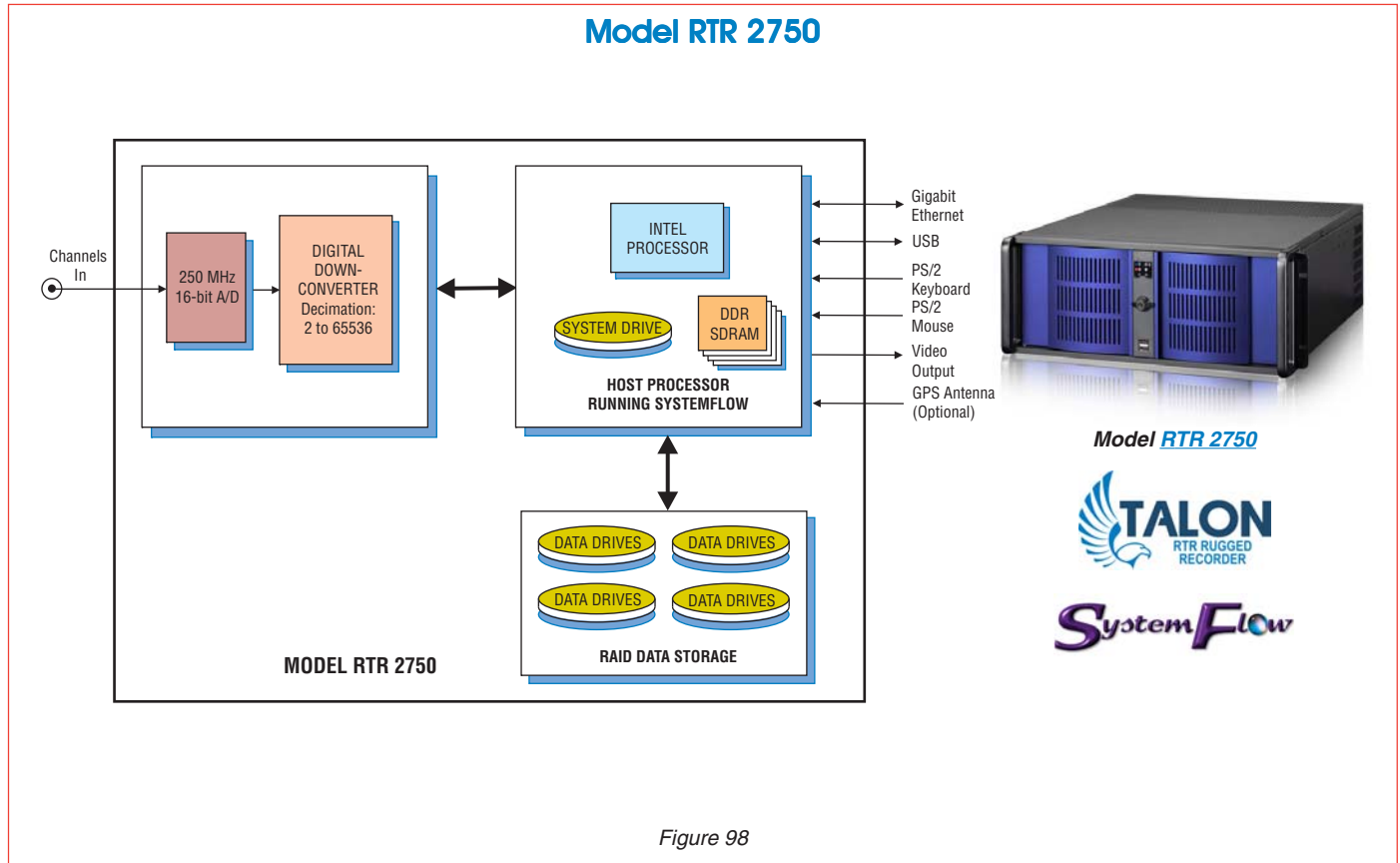
the GUI-selectable system parameters, that provide fully-programmable systems capable of recording and reproducing a wide range of signals.

Included with this system is Pentek's SystemFlow recording software. Built on a Windows 7 Professional workstation with high performance Intel Core i7 processor, the system allows the user to install post-processing and analysis tools to operate on the recorded data. They record data to the native NTFS file system, providing immediate access to the data. Custom configurations can be stored as profiles and later loaded when needed, so users can select preconfigured settings with a single click.

Versions of the [RTR 2726A](#) are also available as a Rackmount Lab unit (Model [RTS 2706](#)), Rugged Rackmount (Model [RTR 2746](#)), and Extreme Rackmount (Model [RTX 2766](#)).

Complementary Products

250 MS/sec RF/IF Rugged Rackmount Recorder



The Talon [RTR 2750](#) is a turnkey recording system that provides phase-coherent recording of 16 independent input channels. Each input channel includes a 250 MHz 16-bit A/D and an FPGA-based digital down-converter with programmable decimations from 2 to 65536, thereby providing the ability to capture RF signals with bandwidths up to 100 MHz.

With options for AC- or DC-coupled input channels, RF signals up to 700 MHz in frequency can be sampled and streamed to disk in real-time at sustained aggregate recording rates up to 8 GB/sec in a 4U rackmount solution.

Designed to operate under conditions of vibration and extended operating temperatures, the [RTR 2750](#) is ideal for military, airborne and field applications that require a rugged system. The hot-swappable solid state storage drives provide the highest level of performance

under harsh conditions and allow for quick removal of mission-critical data.

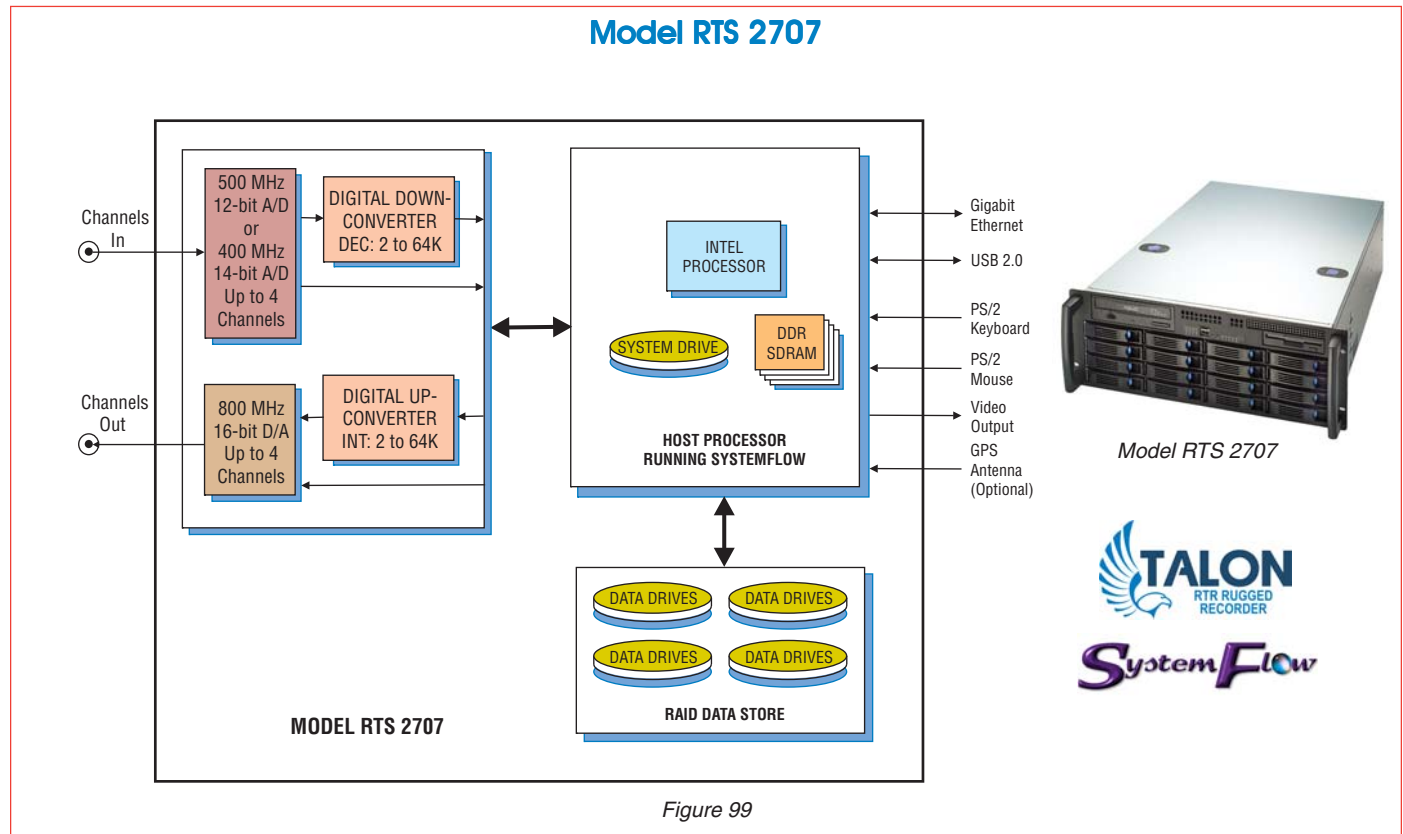
A/D sampling rates, DDC decimations and trigger settings are among the selectable system parameters, providing a system that is simple to configure and operate. An optional GPS time and position stamping facility allows the user to time-stamp each acquisition as well as track the location of a system in motion.

For users who wish to create a custom user interface or to integrate the Talon recording system into a larger application, a C-callable API is also provided as part of SystemFlow. Source code and examples are supplied to allow for a quick and simple integration effort.

Data can be off-loaded through gigabit Ethernet ports or USB 3.0 ports. Additionally, data can be copied to optical disk, using the 8X double layer DVD±R/RW drive.

Complementary Products

500 MS/sec RF/IF Rackmount Lab Recorder



The Talon RTS 2707 is a turnkey, multiband recording and playback system for recording and reproducing high-bandwidth signals. The RTS 2707 uses 12-bit, 500 MHz A/D converters and provides aggregate recording rates up to 1.6 GB/sec.

The RTS 2707 uses Pentek's high-powered Virtex-6-based Cobalt modules, that provide flexibility in channel count, with optional digital downconversion capabilities. Optional 16-bit, 800 MHz D/A converters with digital upconversion allow real-time reproduction of recorded signals.

A/D sampling rates, DDC decimations and bandwidths, D/A sampling rates and DUC interpolations are among the GUI-selectable system parameters, providing a fully-programmable system capable of recording and reproducing a wide range of signals. Optional GPS time and position stamping allows the user to record this critical signal information.

The RTS 2707 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple means to configure and control the recorder.

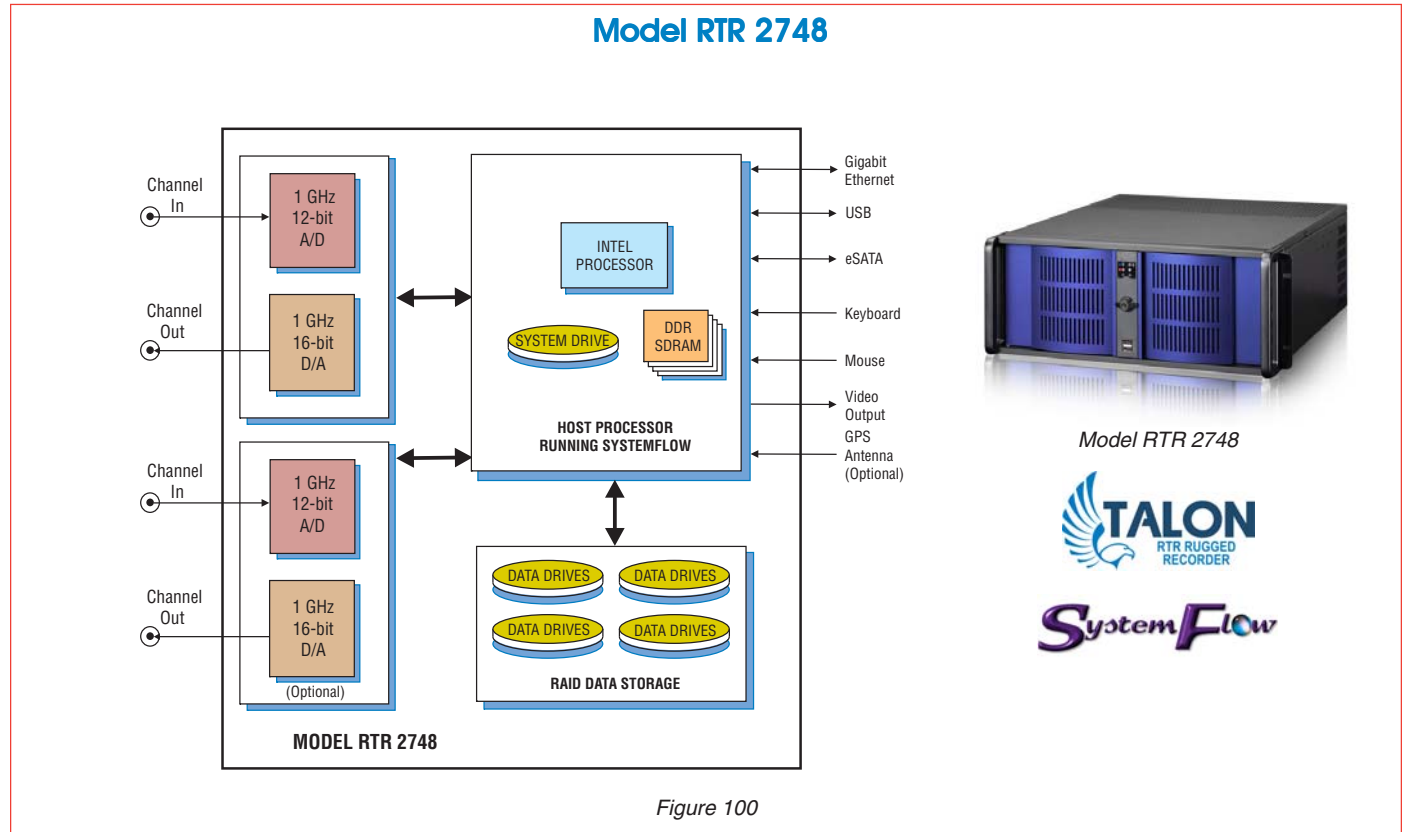
The RTS 2707 is configured in a 4U 19" rack-mountable chassis, with hot-swappable data drives, front panel USB ports and I/O connectors on the rear panel. Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates.

Multiple RAID levels, including 0, 1, 5, 6, 10 and 50, provide a choice for the required level of redundancy. The hot-swappable HDDs provide storage capacities of up to 100 TB in a single 6U chassis.

Versions of the [RTS 2707](#) are available as Rugged Portable (Model [RTR 2727](#)), Rugged Rackmount (Model [RTR 2747](#)), and Extreme Rackmount (Model [RTX 2767](#)).

Complementary Products

1 GS/sec RF/IF Rugged Rackmount Recorder



The Talon RTR 2748 is a turnkey recording and playback system that allows users to record and reproduce signals with bandwidths up to 500 MHz. The RTR 2748 can be configured as a one- or two-channel system to provide real-time aggregate recording and playback rates up to 4.0 GB/sec to an array of solid-state drives.

The RTR 2748 uses Pentek's high-powered Virtex-6-based Cobalt boards that provide the data streaming engine for the high-speed A/D converters. A built-in synchronization module is provided to allow for multi-channel phase-coherent operation. GPS time and position stamping is optionally available.

The RTR 2748 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple means to configure and control the system. Custom configurations can be stored as profiles and later loaded when needed, allowing the user to select preconfigured settings with a single click.

Built on a Windows 7 Professional workstation, the RTR 2748 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTR 2748 records data to the native NTFS file system that provides immediate access to the recorded data.

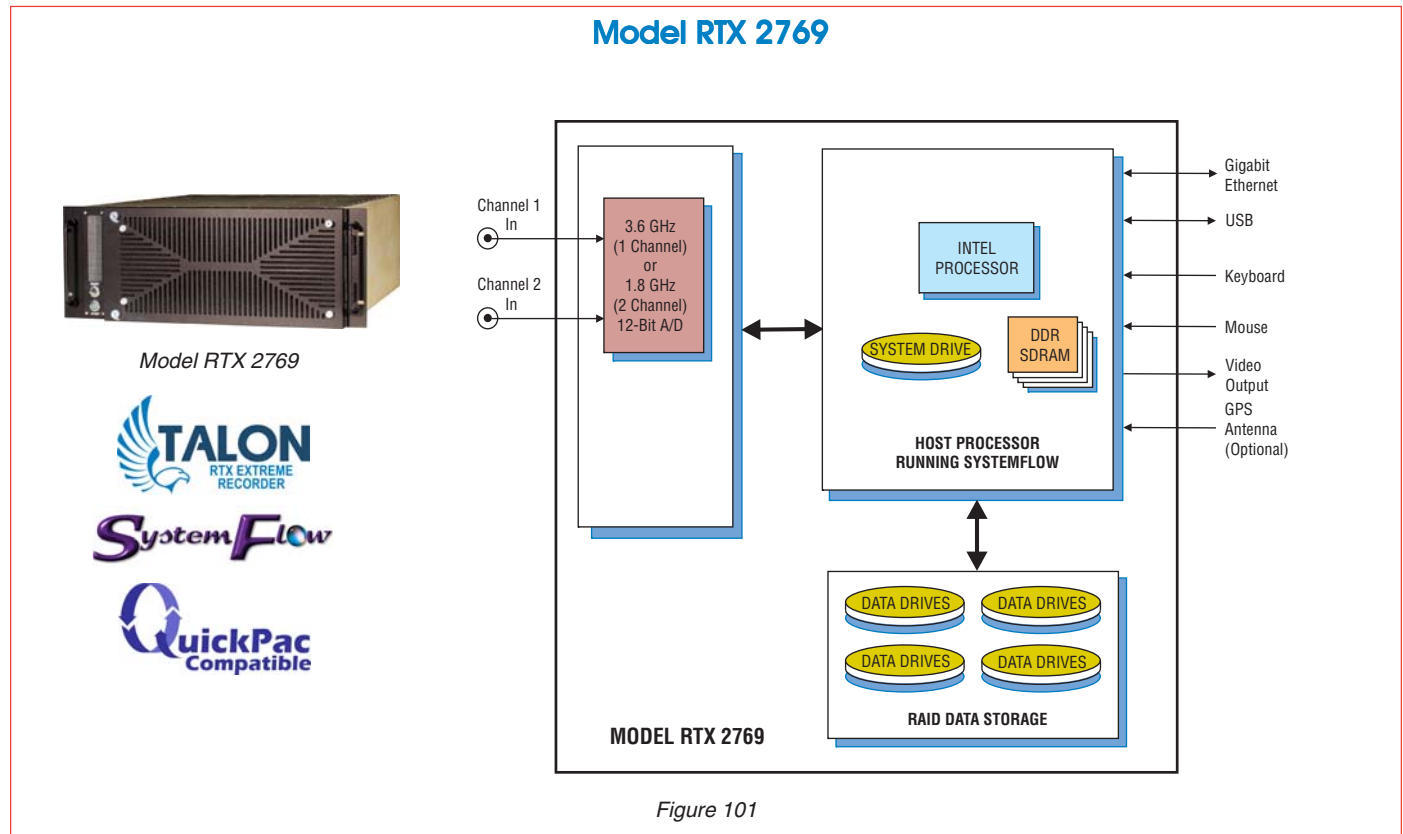
Data can be off-loaded via gigabit Ethernet ports, or USB 2.0 and USB 3.0 ports. Additionally, data can be copied to optical disk, using the 8X double layer DVD±R/RW drive.

Because SSDs operate reliably under conditions of shock and vibration, the RTR 2748 performs well in ground, ship-borne and airborne environments. The drives can be easily removed or exchanged during a mission to retrieve the data.

Versions of the [RTR 2748](#) are also available as a Rugged Portable (Model [RTR 2728](#)), and Extreme Rackmount (Model [RTX 2768](#)).

Complementary Products

3.6 GS/sec Ultra Wideband RF/IF Extreme Rackmount Recorder



The Talon RTX 2769 is a turnkey system that is built to operate under harsh conditions. Designed to withstand high vibration and operating temperatures, the RTX 2769 is intended for military, airborne and UAV applications requiring a rugged system.

Aimed at recording high-bandwidth signals, the RTX 2769 uses 12-bit, 3.6 GHz A/D converters. It can be configured as a one- or two-channel system and can record sampled data, packed as 8-bit- or 16-bit-wide consecutive samples (12-bit digitized samples residing in the 12 MSBs of the 16-bit word). A high-speed RAID array provides an aggregate streaming recording rate to disk of 4.8 GB/sec.

The RTX 2769 uses Pentek's high-powered Virtex-7-based Onyx boards that provide the data streaming engine for the high-speed A/D converters. Channel and packing modes as well as gate and trigger settings are among the selectable system parameters, providing complete control over this ultra wideband recording system.

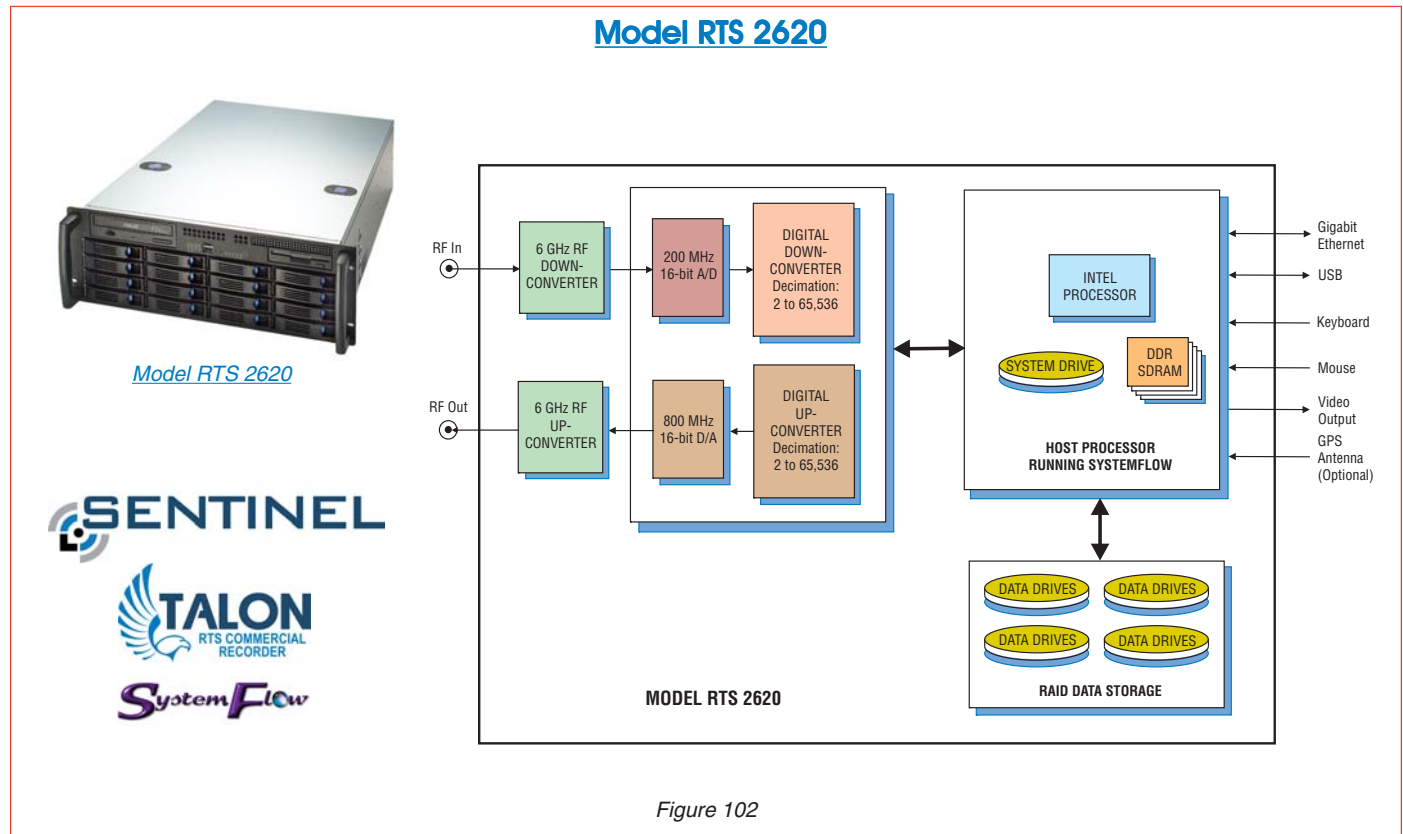
Built on a Windows 7 Professional workstation, the RTX 2769 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTX 2769 records data to the native NTFS file system that provides immediate access to the recorded data.

The Talon RTX 2769 uses a shock- and vibration-isolated inner chassis and solid-state drives to assure reliability under harsh conditions. Developed by Pentek to enhance the operation of Extreme recorders, up to four front-panel removable QuickPac™ drive canisters are provided, each containing up to eight SSDs. Fastened with four thumbscrews, each drive canister can hold up to 7.6 TB of data storage and allows for quick and easy removal of mission-critical data with a minimum of down time.

Versions of the [RTX 2769](#) are available as a Rugged Portable (Model [RTR 2729A](#)), and Rugged Rackmount (Model [RTR 2749](#)).

Complementary Products

6 GHz RF/IF Sentinel Intelligent Signal Scanning Rackmount Recorder



The Talon [RTS 2620](#) combines the power of a Pentek Talon Recording System with those of an RF tuner and RF upconverter hardware plus Pentek's Sentinel Intelligent Signal Scanner. The RTS 2620 provides SIGINT engineers the ability to scan the 6 GHz spectrum for signals of interest and monitor or record bandwidths up to 40 MHz wide once a signal band of interest is detected.

A spectral scan facility allows the user to sweep the spectrum at 30 GHz/sec, while threshold detection allows the system to automatically lock onto and record signal bands. Scan results are displayed in a waterfall plot and can also be recorded to allow users to look back at some earlier spectral activity.

Once a signal of interest is detected, the real-time recorder can capture and store hundreds of terabytes of data to disk, allowing users to store days worth of data. The optional RF upconverter reproduces signals captured at RF frequencies up to 6 GHz.

The Pentek Model [78621](#) Cobalt board transceiver serves as the engine of the [RTS 2620](#) and is coupled with a 6 GHz tuner to provide excellent dynamic range across the entire spectrum. The 200 MHz 16-bit A/D board provides 86 dB of spurious-free dynamic range and 74 dB of SNR.

The Virtex-6-based DDC with selectable decimations of up to 64 k provides exceptional processing gain while allowing users to zoom into signals of varying bandwidths. All system components are integrated into a rackmount chassis that ranges in size from 3U to 6U depending on storage requirements. Front panel removable HDDs, configured as a RAID are hot-swappable and configurable.

An optional GPS receiver and built-in PLLs allow all devices in the RF chain to be locked in phase and correlated to GPS time. GPS position information can optionally be recorded, allowing the recorder's position to be tracked while acquiring RF signals. ➤

Complementary Products

6 GHz RF/IF Sentinel Intelligent Signal Scanning Rackmount Recorder

Model RTS 2620

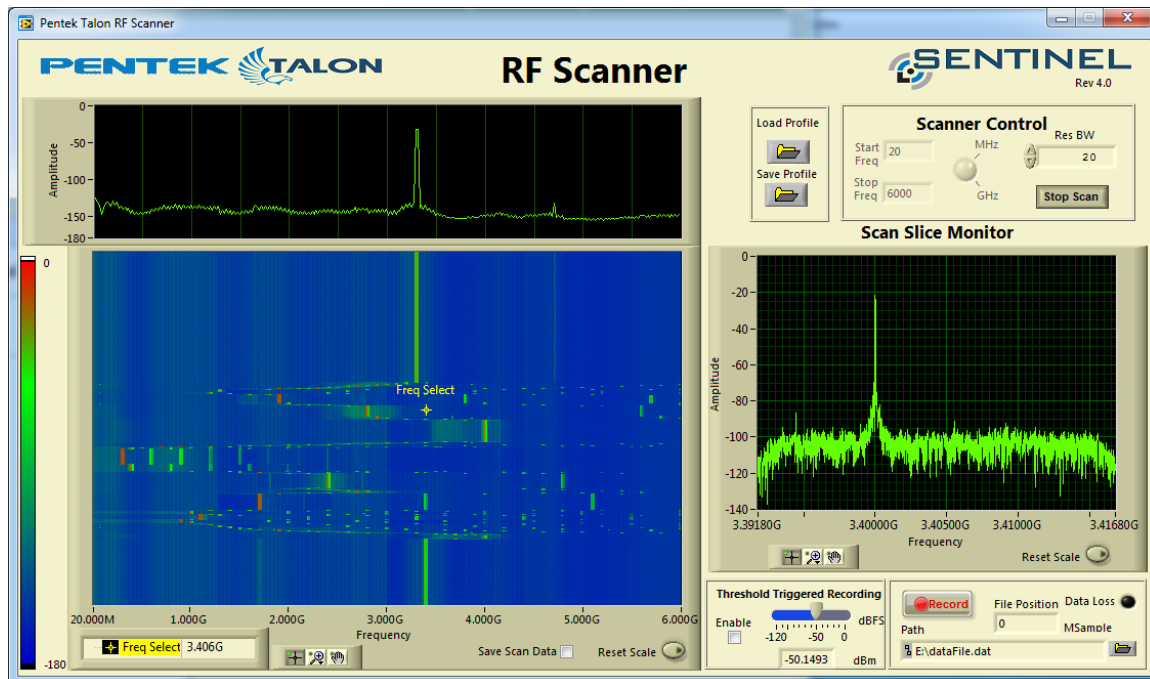


Figure 103

► Pentek's Sentinel™ recorders add intelligent signal monitoring and detection for Talon real-time recording systems. The intuitive GUI allows users to monitor the entire spectrum or select a region of interest, while a selectable resolution bandwidth allows the user to trade sweep rate for a finer resolution and better dynamic range. Scan settings can be saved as profiles to allow for quick setup in the field.

RF energy in each band of the scan is detected and presented in a waterfall display. Any RF band can be selected for real-time monitoring or recording. In addition to manually selecting a band for recording, a recording can be automatically started by configuring signal strength threshold levels to trigger it.

The Sentinel hardware resources are controlled through enhancements to Talon's SystemFlow software package that includes a Virtual Oscilloscope, Virtual Spectrum Analyzer and Spectrogram displays, providing a complete suite of

analysis tools to complement the Sentinel hardware resources.

As shown in the figure above, an RF Scanner GUI allows complete control of the system through a single interface. Start and stop frequencies of a scan can be set by the user as well as the resolution bandwidth. All user parameters can be saved as profiles for easy setup in the field.

Frequency slices from the waterfall display can be selected and monitored, allowing the user to zoom into bands of interest. Threshold triggering levels can be set to record signals that exceed a specified energy. Recordings can also be manually started and stopped.

The Signal Viewer includes a virtual oscilloscope and spectrum analyzer for signal monitoring in both the time and frequency domains. It is extremely useful for previewing live inputs prior to recording, and for monitoring signals as they are being recorded.

Complementary Products

10-Gigabit Ethernet Rackmount Recorder

Model RTS 2715

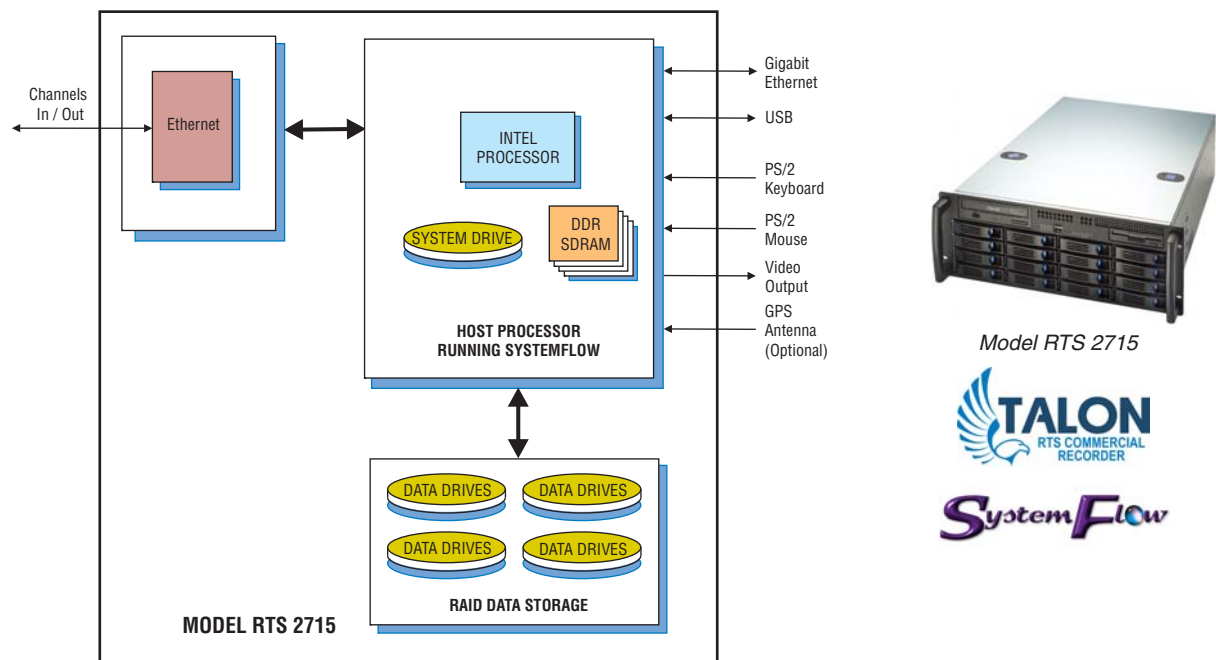


Figure 104

The Talon RTS 2715 is a turnkey rackmount lab recording system for storing one or two 10-gigabit Ethernet (10GbE) streams. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and supports both TCP and UDP protocols. Using highly-optimized disk storage technology, the system achieves aggregate recording rates up to 1.6 GB/sec.

Two rear panel SFP+LC connectors for 850 nm multi-mode or single-mode fibre cables, or CX4 connectors for copper twinax cables accommodate all popular 10 GbE interfaces. Optional GPS time and position stamping accurately identifies each record in the file header.

The RTS 2715 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple and intuitive means to configure and control the system. Custom configurations can be stored as profiles and later

loaded as needed, allowing the user to select preconfigured settings with a single click.

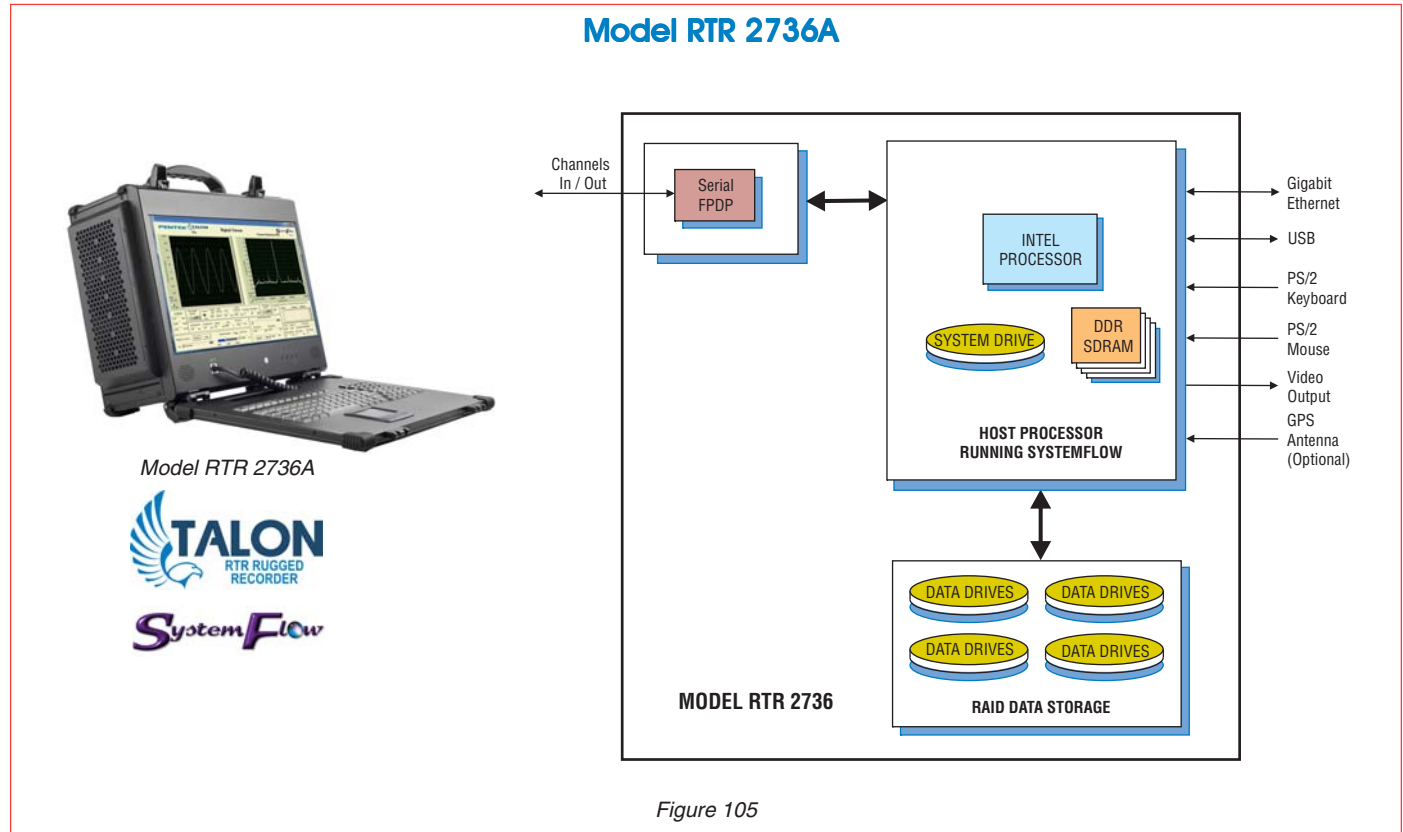
Built on a server-class Windows 7 Professional workstation, the RTS 2715 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTS 2715 records data to the native NTFS file system, providing immediate access to the data.

The RTS 2715 is configured in a 4U or 5U 19" rack-mountable chassis, with hot-swap data drives, front panel USB ports and I/O connectors on the rear panel. Systems are scalable to accommodate multiple chassis to increase channel counts and aggregate data rates.

Versions of the [RTS 2715](#) are also available as Rugged Rackmount (Model [RTR 2755](#)), and Extreme Rackmount (Model [RTX 2775](#)).

Complementary Products

Serial FPDP Rugged Portable Recorder



The Talon RTR 2736A is a complete turnkey recording system designed to operate under conditions of shock and vibration. It records and plays back multiple serial FPDP data streams in a rugged, lightweight portable package. It is ideal for capturing any type of streaming sources including live transfers from sensors or data from other computers and is fully compatible with the VITA 17.1 specification. Using highly-optimized disk storage technology, this system achieves aggregate recording rates up to 3.2 GB/sec.

The system can be populated with up to eight SFP connectors supporting Serial FPDP over copper, single-mode, or multi-mode fiber, to accommodate all popular serial FPDP interfaces. It is capable of receiving and transmitting data over these links and supports real-time data storage to disk. The system is capable of handling 1.0625, 2.125, 2.5, 3.125 and 4.25 GBaud link rates supporting data transfer rates of up to 420 MB/sec per serial FPDP link.

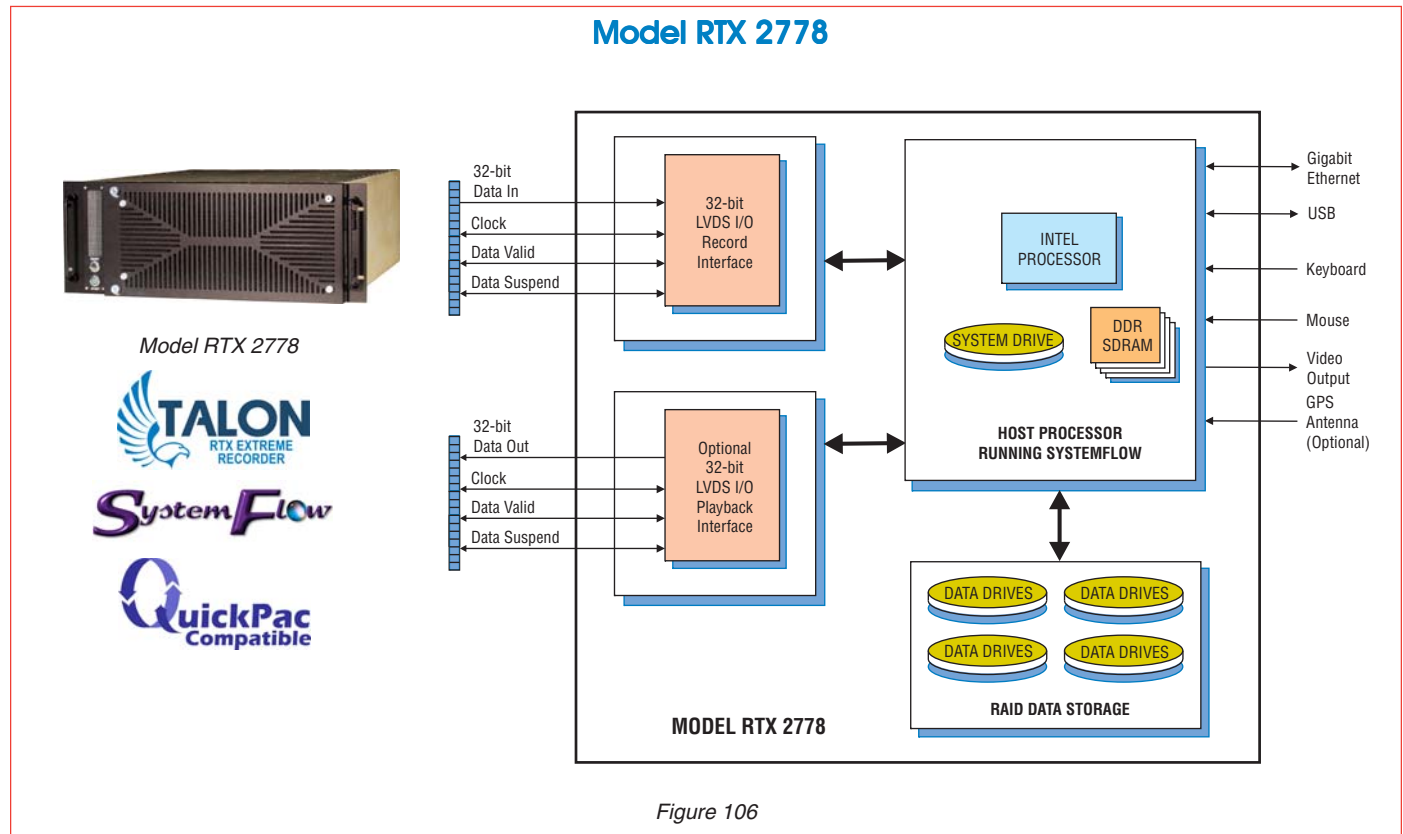
The system includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI that provides a simple and intuitive means to configure and control the system. Custom configurations can be stored as profiles and later loaded as needed, allowing the user to select preconfigured settings with a single click.

The RTR 2736A is configured in portable, lightweight chassis with hot-swap SSDs, front panel USB ports and I/O connections on the side panel. It is built in extremely rugged, 100% aluminum alloy unit, reinforced with shock absorbing rubber corners and impact-resistant protective glass. Using vibration- and shock-resistant SSDs, the system is designed to operate reliably as a portable field system in harsh environments.

Versions of the [RTR 2736A](#) are also available as a Rackmount Lab unit (Model [RTS 2716](#)), Rugged Rackmount (Model [RTR 2756](#)), and Extreme Rackmount (Model [RTX 2776](#)).

Complementary Products

LVDS Digital I/O Extreme Rackmount Recorder



The Talon RTX 2778 is a turnkey record and playback system that is built to operate under harsh conditions. Designed to withstand high vibration and operating temperatures, the RTX 2778 is intended for military, airborne and UAV applications requiring a rugged system.

The RTX 2778 records and plays back digital data using the Pentek Model 78610 LVDS digital I/O board. Using highly optimized disk storage technology, the system achieves aggregate recording rates of up to 1.0 GB/sec.

The RTX 2778 utilizes a 32-bit LVDS interface that can be clocked at speeds up to 250 MHz. It includes Data Valid and Suspend signals and provides the ability to turn these signals on and off as well as control their polarity.

The RTX 2778 includes the SystemFlow Recording Software. SystemFlow features a Windows-based GUI (Graphical User Interface) that provides a simple means to configure and control the system.

Built on a Windows 7 Professional workstation, the RTX 2778 allows the user to install post-processing and analysis tools to operate on the recorded data. The RTX 2778 records data to the native NTFS file system, providing immediate access to the recorded data.

The Talon RTX 2778 uses a shock- and vibration-isolated inner chassis and solid-state drives to assure reliability under harsh conditions. Developed by Pentek to enhance the operation of Extreme recorders, up to four front-panel removable QuickPac™ drive canisters are provided, each containing up to eight SSDs. Fastened with four thumbscrews, each drive canister can hold up to 7.6 TB of data storage and allows for quick and easy removal of mission-critical data with a minimum of down time.

Versions of the [RTX 2778](#) are also available as a Rackmount Lab unit (Model [RTS 2718](#)), Rugged Portable (Model [RTR 2738](#)), and Rugged Rackmount (Model [RTR 2758](#)).

Applications

64-Channel Software Radio Recording System

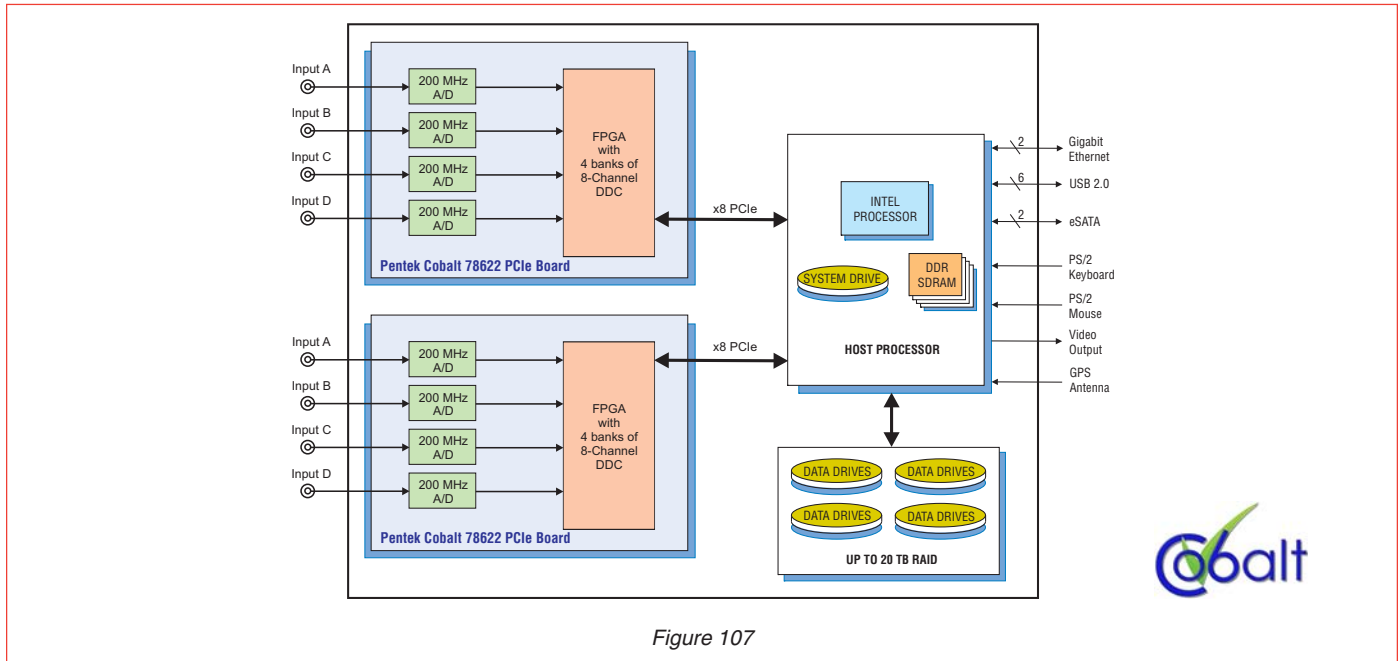


Figure 107

Shown above is a 64-channel recording system utilizing two Pentek Cobalt 78662 PCIe boards. The 78662 samples four input channels at up to 200 megasamples per second, thereby accommodating input signals with up to 80 MHz bandwidth.

Factory-installed in the FPGA of each 78662 is a powerful DDC IP core containing 32 channels. Each of the 32 channels has an independent 32-bit tuning frequency setting that ranges from DC to f_s , where f_s is the A/D sampling frequency. All of the eight channels within each bank share a common decimation setting that can range from 16 to 8192. For example, with a sampling rate of 200 MHz, the available output bandwidths range from 19.53 kHz to 10.0 MHz. Each 8-channel bank can have its own unique decimation setting supporting a different bandwidth associated with each of the four acquisition modules.

The decimating filter for each DDC bank accepts a unique set of user-supplied 18-bit coefficients. The 80% default filters deliver an output bandwidth of $0.8 \cdot f_s / N$, where N is the decimation setting. The rejection of adjacent-band components within the 80% output bandwidth is better than 100 dB.

Each DDC delivers a complex output stream consisting of 24-bit I + 24-bit Q samples at a rate of f_s / N . Any number of channels can be enabled within each bank, selectable from 0 to 8. Each bank includes an output sample interleaver that delivers a channel-multiplexed stream for all enabled channels within a bank.

An internal timing bus provides all timing and synchronization required by the eight A/D converters. It includes a clock, two sync and two gate or trigger signals. An on-board clock generator receives an external sample clock. This clock can be used directly by the A/D or divided by a built-in clock synthesizer circuit.

Built on a Windows 7 Professional workstation with high performance Intel Core i7 processor this system allows the user to install post processing and analysis tools to operate on the recorded data. The system records data to the native NTFS file system, providing immediate access to the recorded data.

Included with this system is Pentek's SystemFlow recording software. Optional GPS time and position stamping allows the user to record this critical signal information.

Applications

L-Band Signal Processing System

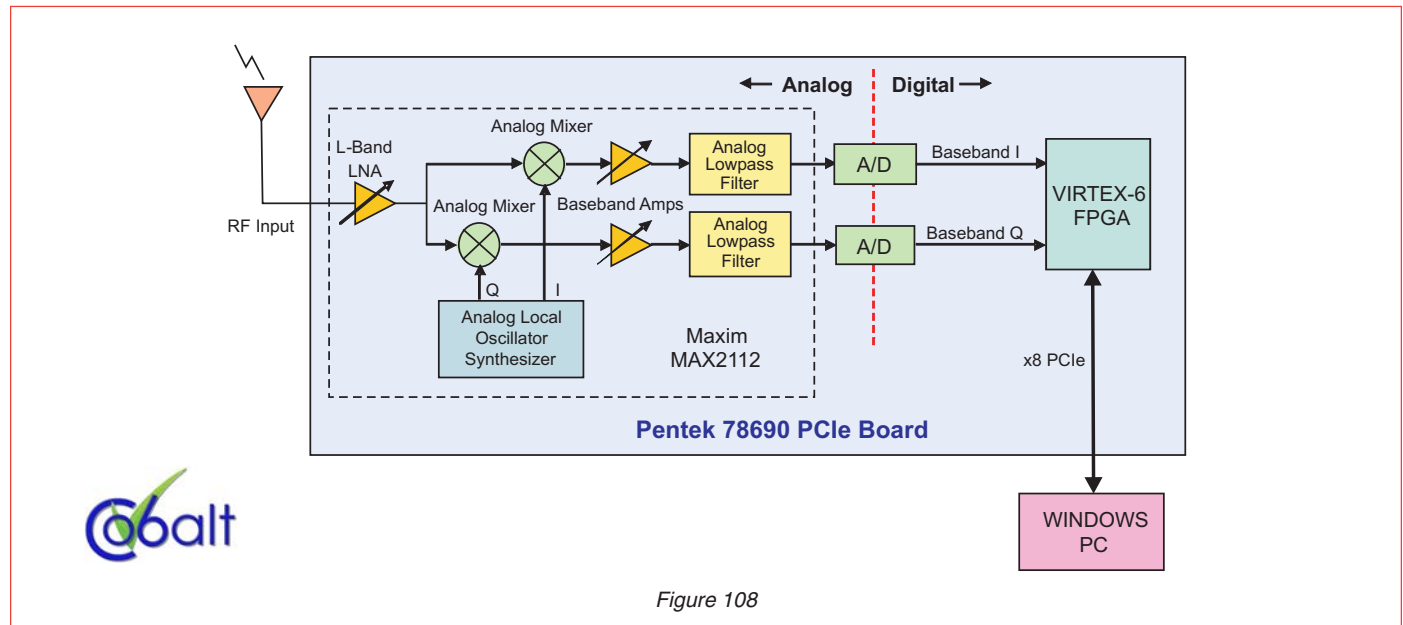


Figure 108

The Cobalt Model 78690 L-Band RF Tuner targets reception and processing of digitally-modulated RF signals such as satellite television and terrestrial wireless communications. The 78690 requires only an antenna and a host computer to form a complete L-band SDR development platform.

This system receives L-Band signals between 925 MHz and 2175 MHz directly from an antenna. Signals above this range such as C Band, Ku Band and K band can be downconverted to L-Band through an LNB (Low Noise Block) downconverter installed in the receiving antenna.

The Maxim Max2112 L-Band Tuner IC features a low-noise amplifier with programmable gain from 0 to 65 dB and a synthesized local oscillator programmable from 925 to 2175 MHz. The complex analog mixer translates the input signals down to DC. Baseband amplifiers provide programmable gain from 0 to 15 dB in steps of 1 dB. The bandwidth of the baseband lowpass filters can be programmed from 4 to 40 MHz. The Maxim IC accommodates full-scale input levels of -50 dBm to +10 dbm and delivers I and Q complex baseband outputs.

The complex I and Q outputs are digitized by two 200 MHz 16-bit A/D converters operating synchronously.

The Virtex-6 FPGA is a powerful resource for recovering and processing a wide range of signals while supporting decryption, decoding, demodulation, detection, and analysis. It is ideal for intercepting or monitoring traffic in SIGINT and COMINT applications. Other applications that benefit include mobile phones, GPS, satellite terminals, military telemetry, digital video and audio in TV broadcasting satellites, and voice, video and data communications.

This L-Band signal processing system is ideal as a front end for government and military systems. Its small size addresses space-limited applications. Ruggedized options are also available from Pentek with the Models 71690 XMC module and the 53690 OpenVPX board to address UAV applications and other severe environments.

Development support for this system is provided by the Pentek ReadyFlow board support package for Windows, Linux and VxWorks. Also available is the Pentek GateFlow FPGA Design Kit to support custom algorithm development.

Applications

8-Channel OpenVPX Beamforming System

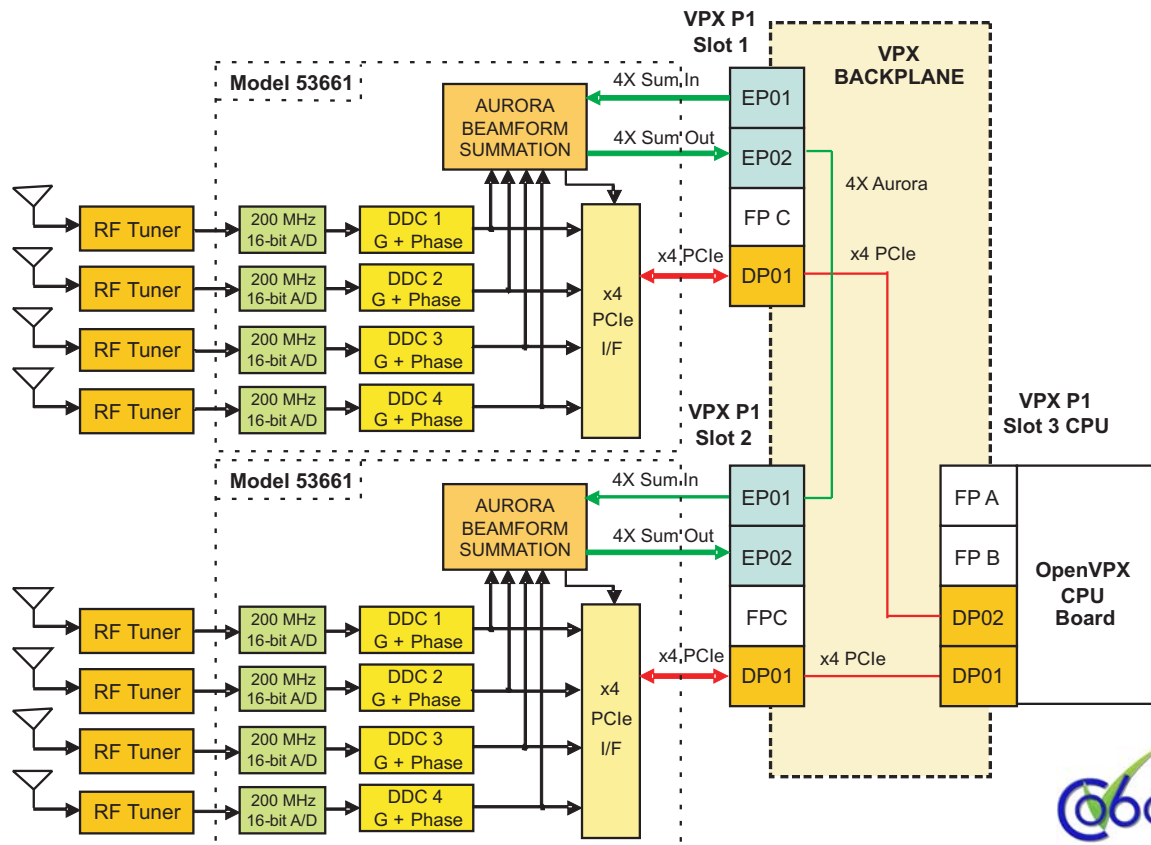


Figure 109

Two Model 53661 boards are installed in slots 1 and 2 of an OpenVPX backplane, along with a CPU board in slot 3. Eight dipole antennas designed for receiving 2.5 GHz signals feed RF Tuners containing low noise amplifiers, local oscillators and mixers. The RF Tuners translate the 2.5 GHz antenna frequency signal down to an IF frequency of 50 MHz.

The 200 MHz 16-bit A/Ds digitize the IF signals and perform further frequency downconversion to baseband, with a DDC decimation of 128. This provides I+Q complex output samples with a bandwidth of about 1.25 MHz. Phase and gain coefficients for each channel are applied to steer the array for directionality.

The CPU board in VPX slot 3 sends commands and coefficients across the backplane over two x4 PCIe links, or OpenVPX “fat pipes”.

The first four signal channels are processed in the upper left 53661 board in VPX slot 1, where the 4-channel beamformed sum is propagated through the 4X Aurora Sum Out link across the backplane to the 4X Aurora Sum In port on the second 53661 in slot 2. The 4-channel local summation from the second 53661 is added to the propagated sum from the first board to form the complete 8-channel sum. This final sum is sent across the x4 PCIe link to the CPU card in slot 3.

Assignment of the three OpenVPX 4X links on the Model 53661 boards is simplified through the use of a crossbar switch which allows the 53661 to operate with a wide variety of different backplanes.

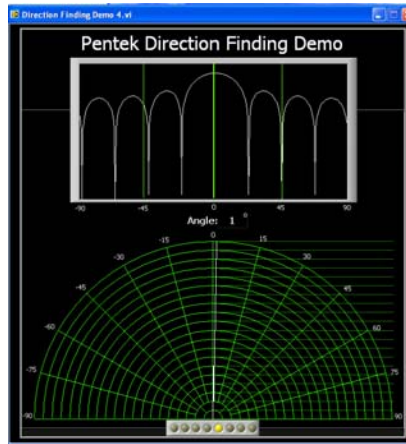
Because OpenVPX does not restrict the use of serial protocols across the backplane links, mixed protocol architectures like the one shown are fully supported. ➤

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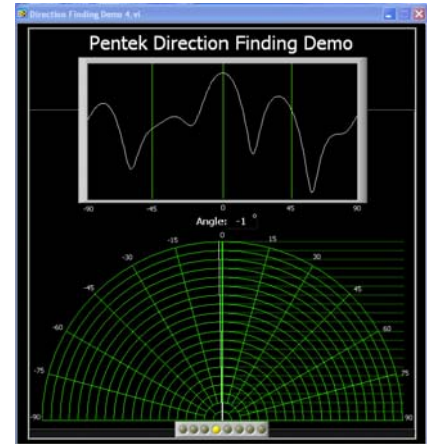
8-Channel OpenVPX Beamforming Demo system



Beamforming Demo Control Panel



Theoretical 7-lobe Beamforming Pattern



Real-Life Beamforming Pattern

Figure 110

► Beamforming Demo System

The beamforming demo system is equipped with a Control Panel that runs under Windows on the CPU board. It includes an automatic signal scanner to detect the strongest signal frequency arriving from a test transmitter. This frequency is centered around the 50 MHz IF frequency of the RF downconverter. Once the frequency is identified, the eight DDCs are set accordingly to bring that signal down to 0 Hz for summation.

The control panel software also allows specific hardware settings for all of the parameters for the eight channels including gain, phase, and sync delay.

An additional display shows the beam-formed pattern of the array. This display is formed by adjusting the phase shift of each of the eight channels to provide maximum

sensitivity across arrival angles from -90° to $+90^\circ$ perpendicular to the plane of the array.

The classic 7-lobe pattern for an ideal 8-element array for a signal arriving at 0° angle (directly in front of the array) is shown above. Below the lobe pattern is a polar plot showing a single vector pointing to the computed angle of arrival. This is derived from identifying the lobe with the maximum response.

An actual plot of a real-life transmitter is also shown for a source directly in front of the display. In this case the perfect lobe pattern is affected by physical objects, reflections, cable length variations and minor differences in the antennas. Nevertheless, the directional information is computed quite well. As the signal source is moved left and right in front of the array, the peak lobe moves with it, changing the computed angle of arrival.

This demo system is available online at Pentek. If you are interested in viewing a live demonstration, please let us know of your interest by clicking on this link:

[Beamforming Demo.](#)